

Low Power Secure Digital Host Controller



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ABSTRACT

LOW POWER SECURE DIGITAL HOST CONTROLLER

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With the increasing consumer digital content, demand for high capacity digital storage is increasing rapidly. Today, portable storage media's are widely used in all mobile phones, digital cameras, camcorders, and in many multimedia devices. Different memory formats like Flash, Secure Digital (SD), Compact Flash, Universal Serial Bus (USB), and Multimedia Card (MMC) are available in the market to store the digital contents. Of all these formats, SD provides many advantages over other formats. SD cards provide high storage capacity, higher transfer speed, and interoperability with Personal Computer (PC) - related devices and multimedia products.

Portable devices are battery operated, so they need to be power efficient. The goal of the project is to design low power SD host controller. The SD host controller consumed total power of 1.162mW. This was achieved by using low power design techniques, right set of synthesis tools, technology library, and constraints.

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Table of Content

1.0	Introduction.....	1
1.1	Project Scope	2
2.0	Literature Review	3
2.1	Introduction.....	3
2.2	Process Scaling	4
3.0	Low Power Techniques	9
3.1	Clock Gating	9
3.2	Gate Level Power Optimization.....	9
3.3	Voltage and Frequency Scaling	10
3.4	Multi-VDD.....	10
3.5	Multi-VT (Threshold Voltage)	11
4.0	Architecture of SD Host Controller	13
4.1	Key Features	13
4.2	SD Host Controller Block Diagram.....	13
4.3	SD Controller Interface Signals	15
5.0	SD Standard Register Map	18
5.1	SD Host Controller Register Map.....	19
6.0	SD Protocol.....	20
6.1	SD BUS Protocol	21
6.2	Data Packet Format.....	22
6.3	SD Command Format	23
7.0	Low Power Implementation.....	27
7.1	Software Power management	27
7.2	Clock Gating and Voltage Scaling.....	29
7.3	Multi Vt Optimization.....	31
8.0	Economic Justification	33
8.1	Executive Summary	33
8.2	Problem Statement	34
8.3	Solution & Value Proposition.....	34
8.4	Market Size	35

8.5	Competitors.....	38
8.6	Customers	38
8.7	Cost.....	39
8.8	Price Point.....	40
8.9	Personnel.....	40
8.10	SWOT	41
8.11	Business & Revenue Model.....	41
8.12	Exit strategy	42
8.13	Cash Flow Analysis	43
9.0	Break-Even Analysis.....	46
10.0	Return on Investment (ROI).....	48
11.0	Synthesis and Simulation Results.....	50
12.0	Future Work.....	50
13.0	Conclusion	50
	References.....	52
	Appendix A.....	53
	Appendix B.....	65
	Appendix C.....	72

List of Figures

Figure 1: Power Dissipation Vs Year	1
Figure 2 : Intel 4004 CPU Interior	4
Figure 3 : Moore's Law	5
Figure 4 : Trend of MOS Logic Technologies.....	6
Figure 5: Inverter Dynamic Power	7
Figure 6 : Leakage Power	8
Figure 7: Gate Level Power Optimization	9
Figure 8 : Multi VDD Power Optimization	11
Figure 9 : Multi- Threshold Voltage Technique.....	11
Figure 10 : SD Host Controller Block Diagram	13
Figure 11 : SD Standard Register Map.....	18
Figure 12: SD BUS Protocol.....	21
Figure 13: SD Command Frame	21
Figure 14 : Response Frame	22
Figure 15: Data Packet Format for Standard Bus	22
Figure 16: Data Structure in 4-bit Mode.....	23
Figure 17 : SD Command Format.....	23
Figure 18: SD Common Initialization Routine.....	25
Figure 19: SD Data Transfer Flow.....	26
Figure 20: SoC System with SD Host Controller	27
Figure 21: CPM Register	28
Figure 22: Simulation showing Clock cut off when there is not data transfer	28
Figure 24: SD Market Size	35
Figure 25: Products using SD format to store digital content.....	36
Figure 26: Mobile Phone Market with SD Cards	36
Figure 27: Mobile Phone Market.....	37

Figure 28: Worldwide Smartphone Sales	37
Figure 29 : Mobile Device Vendor Market Share	39
Figure 30: Revenue and Total Cost of the Company.....	44
Figure 31: Break Even Analysis	47
Figure 32: Profit and Loss Chart.....	47
Figure 33: Return on Investment	49

List of Tables

Table 1: AHB Interface Signals.....	15
Table 2: Power Signals	15
Table 3 : SD Card Interface Signals	16
Table 4: RAM Interface Signals	17
Table 5: SD Host Controller Register Map.....	19
Table 6 : SD Card Interface	20
Table 7: Dynamic Power (MW/MHz)	30
Table 8: Leakage Power (MW).....	30
Table 9: Total Power (mW)	31
Table 10: Total Power with Multi-Threshold Voltage (mW).....	31
Table 11: Project Schedule	32
Table 12: SWOT Analysis	41
Table 13: Units sold by the Companies	43
Table 14: Cash Flow Analysis	44
Table 15: Calculation of Variable Cost	45
Table 16: Calculation of Total Income	45
Table 17: Break Even Analysis.....	46
Table 18: Calculation of ROI.....	48

1.0 Introduction

In today's era of technology and communication, adding new features in a product while maintaining its performance is a great challenge. The storage devices for the next-generation design will play central role in the consumer electronics market including personal devices, communication and entertainment. The power has been the second criteria for the semiconductor industries after other issues such as performance, cost, and area. To design the devices as per customer's requirements with low cost and low power is becoming the major challenge for the developers. Figure 1 shows how the power dissipation is increasing exponentially after 1998. Before 1998 the power increment was in a straight line. Power budget increment can fail the project. Excessive power density can also reduce the reliability (Kneating M. et el, 2007). Low power product reduces the power dissipation, and hence, the cost of thermal management.

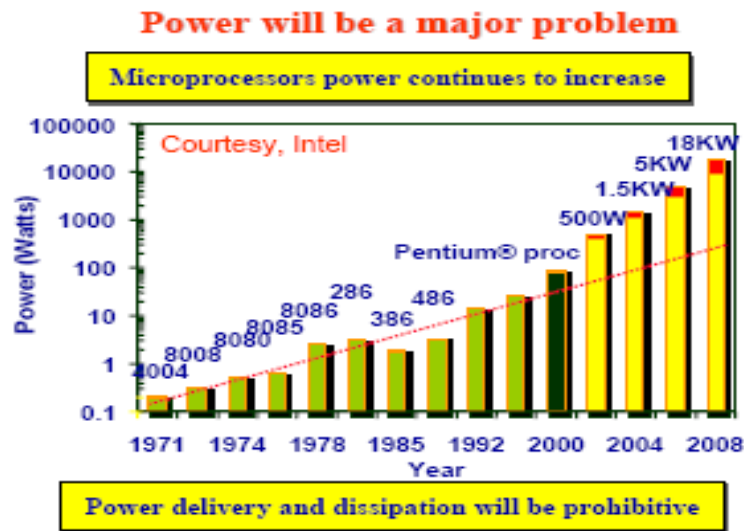


Figure 1: Power Dissipation Vs Year

Source: Thuy Le. *Advanced Digital System Design & Synthesis* (PDF document). Retrieved from <http://www.engr.sjsu.edu/tle/271.html>

To store information digitally, different types of formats and memory cards are being developed. Compact Flash, Smart Media were some of the formats that were popular from 2001 to 2004. Today, Secure Digital (SD) cards and memory sticks are taking the sweet spot for storing digital information. SD memory cards are widely used in digital cameras, digital camcorders, mobile phones, personal digital assistants, GPS receivers, and video games. Secure Digital card popularly known as SD card is very small in size (size of postage stamp) and can store high quality error free digital data with high level protection built into each card. Standard SD card capacity ranges from 1 MB to 4 GB. Change in technology allows more storage capacity in secure digital cards, named Secure Digital High Capacity (SDHC), Secure Digital eXtended Capacity (SDXC), and Secure Digital Input Output (SDIO). They have storage capacity from 1 MB TO 2 TB. SD card provides fast speed, low-power operation, easy storage and accesses.

The main focus of the project is to design a low power, high performance standard SD Host Controller for SD cards. Power consumption reduction increases the battery life in addition to better performance for any portable device. There are different types of power reduction techniques used in the industry such as voltage scaling, clock gating, power gating, transistor scaling, adiabatic circuits, technology scaling, transition reduction, parallelism, etc. (Paring T., and Bowers H., 1996). By using proper set of synthesis tools and libraries the power can be extensively reduced without affecting the performance.

1.1 Project Scope

The objective of MS Inc. is to design low power SD Host Controller. The product will conform to SD Host Controller Standard Specification Version 2.0. The goal is to reduce the power by at least 20% compare to the same product available in the market.

2.0 Literature Review

The objective of this project is to design a low power Secure Digital Host Controller IP core. The various market trends in the semiconductor industry were analyzed to validate the need for and the viability of this product. The most common low power design techniques were researched and those that could be applied to this project were identified. The literature review is done through extensive research from journals, books, online encyclopedia and discussion with industrial professionals.

2.1 Introduction

Portable storage devices are becoming popular and growing rapidly. These devices can store and acquire information wherever whenever you need. The important applications of portable storage devices are to make backup copies of important data, to share information between different computers or persons, to store digital pictures, music, games, power point presentations etc., and to secure information. These devices are very cost effective, easy to use, and extremely practical.

Secure Digital (SD) cards are designed for portable storage applications. They have many advantages over their predecessors. They have high storage capacity and built upon NAND flash technology. SD cards have security feature built in for protecting digital contents. These devices are battery operated and have to be power efficient. Historically power was not a constraint but today there is an increasing demand for low power devices. Power supply constraints, board and system level thermal challenges, overall system cost and ecological benefits are some of the reasons to call for low power designs.

There are many techniques available today to reduce power in the digital circuits such as voltage scaling, power gating, clock gating and so on. By reducing supply voltage, we can reduce significant power consumption in the components of the circuit and as in the whole circuit. This document outlines approaches that have been carried out in the history of designing low power circuits and storage devices.

2.2 Process Scaling

In 1968, Bob Noyce and Gordon Moore left Fairchild Semiconductor to start their own company focusing on building products using integrated circuits. They named their company Intel. In 1969, Intel received contract to design chips for desktop calculator. Intel conceived idea of creating a general purpose processor chip that would read instructions from a memory chip. Eventually this became the first microprocessor. In November, 1971, Intel had publicly introduced the world's first single chip microprocessor, the Intel 4004 with just over 2,300 transistors in an area of only 3 by 4 millimeters (Bellis, 1997).

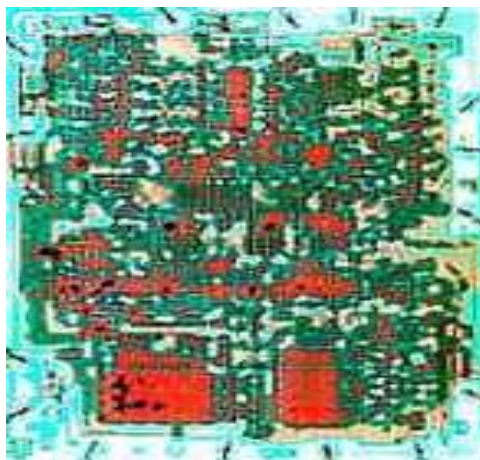


Figure 2 : Intel 4004 CPU Interior

Source: Bellis M. (1997), *Inventors of the Modern Computer*. Retrieved October 1, 2009, from About.com website: <http://inventors.about.com/od/mstartinventions/a/microprocessor.ht>

With increase in demand for high speed processors, power dissipation by processor also increased. Concerns over power consumptions became high priority. Scaling down MOS devices was one of the techniques used to bring down power supply voltage. This reduced gate delay by 30%, reduced power by 50% and allowed clock frequency to increase up to 43% (White & Chen, 2008). According to Moore's law, number of transistors on integrated circuit doubles every two years. This law is very well illustrated in the Figure which shows the number of transistors for Intel processors from 1970 to 2007.

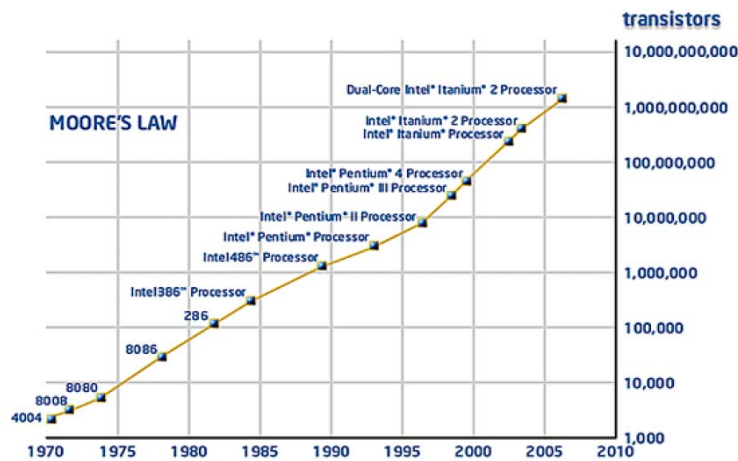


Figure 3 : Moore's Law

Source: White, M., & Yuan, C. (2008, 3). Scaled CMOS Technology Reliability User Guide. Retrieved April 15, 2009, from National Aeronautics and Space Administration website: <http://parts.jpl.nasa.gov/docs/NEPP07/NEPP07ScaledCMOSTechnologyReliabilityUsersGuide.pdf>

The figure 4 shows how power supply voltage and threshold voltage tend to change with process scaling technology.

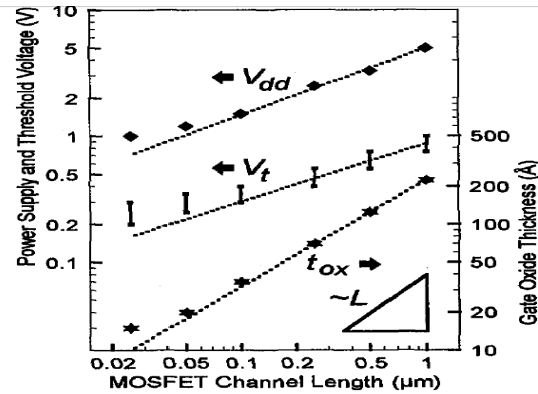


Figure 4 : Trend of MOS Logic Technologies

Source: White M., & Chen Y. (2008), Scaled CMOS Technology Reliability Users Guide. Retrieved on October 06, 2009 from website: <http://parts.jpl.nasa.gov/docs/NEPP07/NEPP07/ScaledCMOSTechnologyReliabilityUsersGuide.pdf>

As the technology has shrunk, in the deep submicron from 90nm technology, more and more numbers of gates are being placed in small size of chip. This has led to a problem towards the leakage current and power dissipation. Packaging and cooling are becoming more and more complex in deep submicron technology. Reliability also decreases, as the power density goes up because mean time of failure decreases exponentially with temperature.

The leakage of deep submicron process has a major effect on battery operated device. According to ITRS battery life has decreased after 2004 as more and more features have been added. Designers are taking different approaches towards each step of the design process from software to implementation. The different techniques such as clock gating, power gating, multi-VT, multi-voltage, etc. are the approaches taken by the designers to reduce the power.

The total power is the sum of

- Dynamic Power
- Leakage Power

Dynamic Power:

It is the power drawn by the circuit when it is operating due to the system activity and switching.

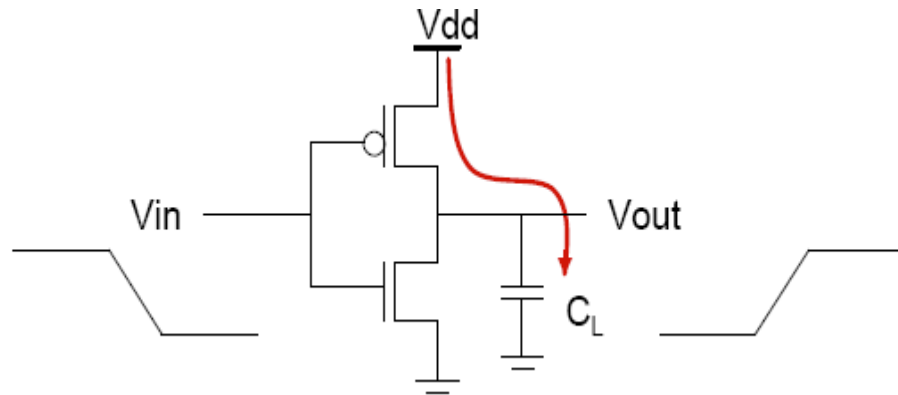


Figure 5: Inverter Dynamic Power

Source: Kneating M., Flynn D., Aitken R., Gibbons A., & Shi K. (2007). Low power methodology manual (LPMM).

In the above circuit, when the input is low the output is high and charges the load capacitor C_L . Similarly, when the input is high the output is low and discharges the capacitor. Most of the power dissipation is during charging and discharging of this capacitance. This power is called dynamic power and is given by,

$$\text{Dynamic power } P = C_L V_{dd}^2 f$$

Where C_L is the load capacitance, V_{dd} is the supply voltage, and f is the clock signal frequency.

Leakage Power:

This is the static power drawn by the circuit when it is powered up but all its clocks are switched off and held at a constant voltage. Leakage power is independent of the transition or any switching activity and hence, it is constant. Leaky transistors and diodes are the main causes of the leakage power.

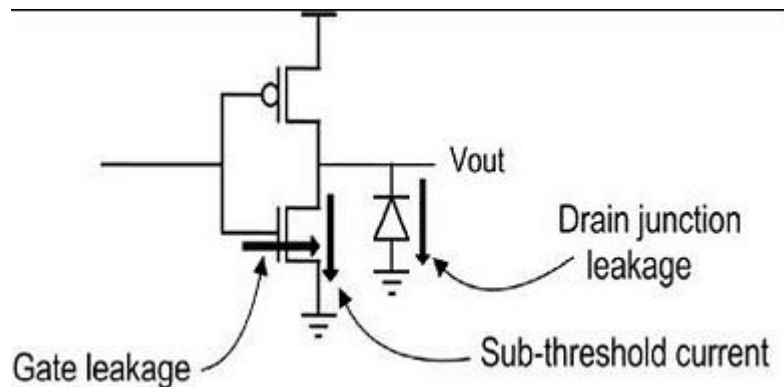


Figure 6 : Leakage Power

Source: Kneating M., Flynn D., Aitken R., Gibbons A., & Shi K. (2007). Low power methodology manual (LPMM).

$$P_{\text{leak}} = V_{\text{dd}} * I_{\text{leak}}$$

Where P_{leak} is the leakage power, V_{dd} is the supply voltage and I_{leak} is the leakage current.

Sub-threshold current occurs when the gate is not turned off completely. The Gate leakage current occurs as a result of tunneling current through the oxide gate.

3.0 Low Power Techniques

Several low power techniques have been and being used by the designers to reduce the power. The different techniques are

- Clock Gating
- Gate level power optimization
- Voltage and Frequency Scaling
- Multi-VDD
- Multi-VT

3.1 Clock Gating

The most common way to reduce power is to turn off the clock when it is not required.

Pokhrel and his team from Synopsys Inc., recently compared design with clock gating circuit and without clock gating. Their reports indicate area reduction of 20% and power savings of 34%.

Earlier Register Transistor Logic (RTL) designers used to code clock gating circuits explicitly in the RTL. Today Synthesis tool include libraries with clock gating cells (Pokhrel, 2007).

3.2 Gate Level Power Optimization

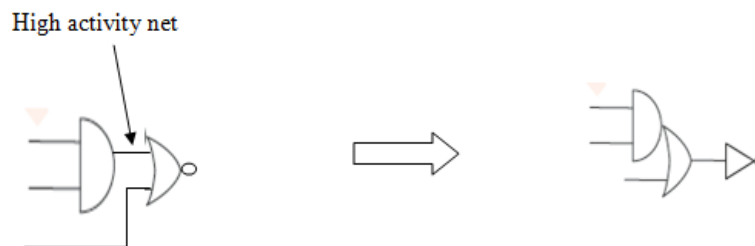


Figure 7: Gate Level Power Optimization

Source: Kneating M., Flynn D., Aitken R., Gibbons A., & Shi K. (2007). Low power methodology manual (LPMM).

Optimization of logic by synthesis tool is one the technique to reduce dynamic power. In figure 7, output of the AND gate which is a high activity net is connected to “NOR” gate. With Low power option, the synthesis tool can re-arrange logic such that the high activity net becomes internal to the cell driving a much smaller capacitance thereby reducing dynamic power (Kneating M. et el, 2007).

3.3 Voltage and Frequency Scaling

In CMOS circuit, the dynamic power is largely described by the equation:

$$P_{\text{dyn}} = C \times V_{\text{dd}}^2 \times f$$

Where P_{dyn} is dynamic power, C is the capacitance, V_{dd} is the supply voltage and f is the clock frequency.

Reducing the supply voltage and clock frequency based on work load is one of the techniques for reducing dynamic power. This technique will improve battery lifetime significantly.

3.4 Multi-VDD

As shown in above equation, dynamic power is proportional to V_{dd}^2 . The power reduces significantly by lowering V_{dd} on selected blocks. In figure 8, the RAMS run at the highest voltage as they are on the critical path of timing. But the voltages on other blocks can be reduced without affecting the overall performance (Kneating M. et el, 2007).

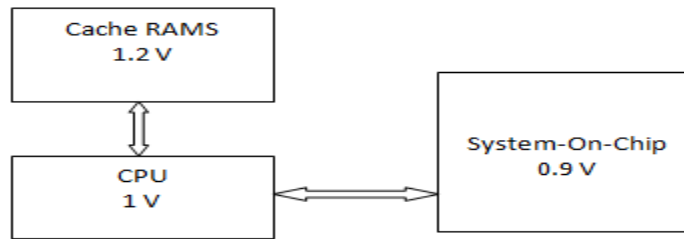


Figure 8 : Multi VDD Power Optimization

Source: Kneating M., Flynn D., Aitken R., Gibbons A., & Shi K. (2007). Low power methodology manual (LPMM).

3.5 Multi-VT (Threshold Voltage)

Using technology libraries with multiple threshold logic V_T can reduce leakage current. Implementation tools can use these libraries to optimize timing and power simultaneously. There are three versions of the cells: LVT (Low Voltage Threshold), SVT (Standard Voltage Threshold), and High Voltage Threshold). Figure 9 shows the relationship between leakage and delay for 90 nm technology for these versions.

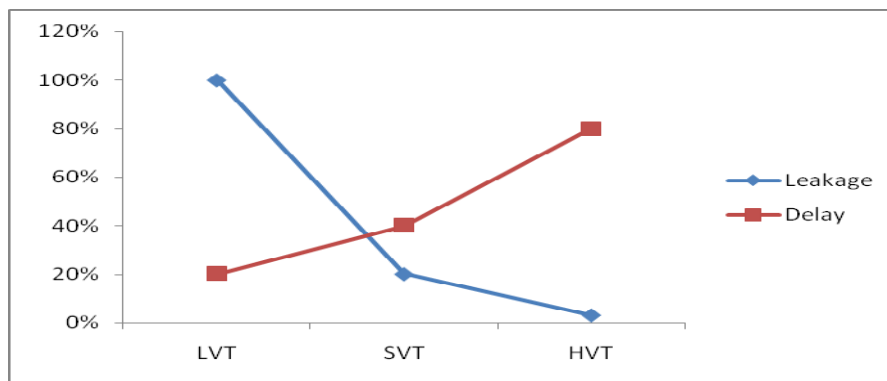


Figure 9 : Multi- Threshold Voltage Technique

Source: Kneating M., Flynn D., Aitken R., Gibbons A., & Shi K. (2007). Low power methodology manual (LPMM).

The goal of this technique is to reduce the number of leaky transistors by positioning them only when necessary to meet timing. First the synthesis is done by using primary library and then optimizing the additional library/libraries with different VT (Kneating M. et el, 2007).

Increasing awareness of global warming and green technology is fueling the rise of low power's importance. Low power has become very essential for circuit design today, driven by the increasing complexity and operating speeds of microprocessors and the demands of portable electronic equipment. The sudden increase in the popularity of cell phones, MP3 players, PDAs and other handheld systems has made extended battery life a major selling point for portable systems (Donlin, 2008).

Secure Digital Host Controller will be designed based on low power techniques. The design will be partitioned to support low power techniques, especially power gating. Implementation of clocks and reset signal will follow, keeping low power in mind. Features to support software to control power management logic will be devised to save overall power consumption.

4.0 Architecture of SD Host Controller

4.1 Key Features

- Supports one SD Slot , Supports 1-bit and 4-bit operational modes
- Compliant with SD Host Controller Standard Specification Version 2.0
- AMBA Bus Host Interface
- Supports Advance DMA mode
- Cyclic Redundancy Check CRC7 for Command and CRC16 for Data
- Built in 1K FIFO for efficient data transfer with Host CPU
- Support Interrupts
- Upto 200 Mbits data transfer rate at 50MHz in 4-bit parallel mode

4.2 SD Host Controller Block Diagram

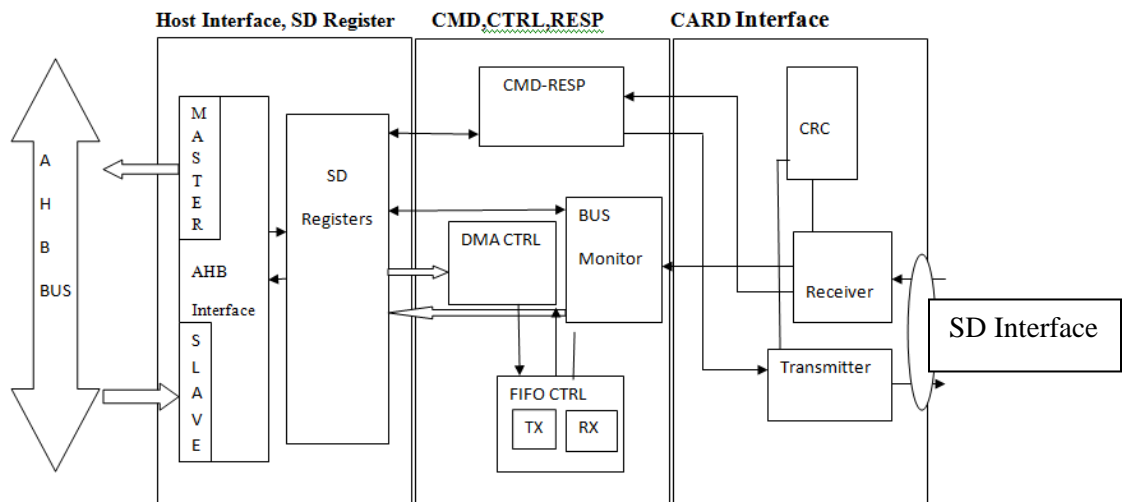


Figure 10 : SD Host Controller Block Diagram

SD Host Controller is designed keeping low power in mind. It is been architecture to have control over power management based on its application in different SoC designs. The design is partitioned into following sections:

Host Interface:

Host interface connects the AHB Master and Slave to AHB bus. In order to setup a command the host communicates with SD Register through slave interface. The SD controller Master interface is used for DMA Data to/from host memory.

Controller:

The CMD and RESP block initiates CMD to the card and receives response from the card and update SD registers. DMA CTRL block controls the DMA transfer to/from Host memory. The BUS Monitor looks for protocol violation and update SD status registers. FIFO (First-In First-Out) CTRL manages the TX and RX FIFO's during transmission and reception and act as a flow control during read and write data transfers.

Card Interface:

Card Interface consists of transmitter and receiver block that interacts with the physical interface of the SD card. Command and Data uses CRC checker (CRC7 and CRC16).

4.3 SD Controller Interface Signals

4.3.1 AHB Interface Signals

Table 1: AHB Interface Signals

Signal	Direction	Description
Clk_ahb	IN	AHB System Clock
M_mbusreq	OUT	AHB Bus request
M_hgrant	IN	AHB Bus Grant
M_haddr[31:0]	OUT	Address bus
M_hwdata[31:0]	OUT	AHB master write data
M_hrdata[31:0]	IN	AHB master read data
M_hwrite	OUT	Write/Read signal
M_hsize[2:0]	OUT	Size(byte, half word or word)
M_hburst[2:0]	OUT	Burst Size
M_hready	IN	Ready signal
M_htrans[1:0]	OUT	Transfer type
M_hresp[1:0]	IN	Transfer response
Intr	OUT	Interrupt to the Host
T_hsel	IN	Slave Select
T_haddr[31:0]	IN	Slave address
T_hwdata[31:0]	IN	Slave write data
T_hrdata[31:0]	OUT	Slave read data
T_hwrite	IN	Slave write/read signal
T_hsize[2:0]	IN	Size
T_htrans[1:0]	IN	Transfer type
T_hready	OUT	Slave ready
T_hresp[1:0]	OUT	Transfer Response

4.3.2 Power Signals

Table 2: Power Signals

Signal	Direction	Description
bus_pow_s1	OUT	Control SD Card Power Supply
bus_volt_s1[2:0]	OUT	SD Bus voltage select
bus_volt_s1[2:0]	OUT	SD Bus voltage select

4.3.3 SD Card Interface Signals

Table 3 : SD Card Interface Signals

Signal	Direction	Description
Clk_sdcard_out	OUT	SD Clock
Clk_sdcard_in	IN	Feed Back of clk_sdcard_out
CMD	INOUT	CMD/RESPONSE
CMD_IN	IN	SD1/SD4: CMD input
CMD_OUT	OUT	SD1/SD4:CMD output
CMD_OUT_EN	OUT	CMD output Enable
DATA0	INOUT	DATA0
DATA0_IN	IN	DATA0 Input
DATA0_OUT	OUT	DATA0 Output
DATA0_OUT_EN	OUT	DATA0 Output Enable
DATA1	INOUT	DATA1
DATA1_IN	IN	DATA1 Input
DATA1_OUT	OUT	DATA1 Output
DATA1_OUT_EN	OUT	DATA1 Output Enable
DATA2	INOUT	DATA2
DATA2_IN	IN	DATA2 Input
DATA2_OUT	OUT	DATA2 Output
DATA2_OUT_EN	OUT	DATA2 Output Enable
DATA3	INOUT	DATA3
DATA3_IN	IN	DATA3 Input
DATA3_OUT	OUT	DATA3 Output
DATA3_OUT_EN	OUT	DATA3 Output Enable
SDCD	IN	Card Detect
SDWP	IN	Card Write Protect
Clk_ram	OUT	Clock to RAM
Clk_xin	IN	SD clock input to generate SD clock
Rstahb_n	IN	External Reset

4.3.4 External RAM Interface Signals:

Table 4: RAM Interface Signals

Signal	Direction	Description
AA[7:0]	OUT	Address to Port A for FIFO
DA[7:0]	OUT	Write data to Port A for FIFO
CENA	OUT	Active low Chip Enable to Port A for FIFO
WENA	OUT	Active low Write Enable to Port A for FIFO
BYTEENA[3:0]	OUT	Active low Byte Enable to Port A for FIFO
AB[7:0]	OUT	Address to Port B for FIFO
DB[7:0]	OUT	Write data to Port B for FIFO
CENB	OUT	Active low Chip Enable to Port B for FIFO
WENB	OUT	Active low Write Enable to Port B for FIFO
BYTEENB[3:0]	OUT	Active low Byte Enable to Port B for FIFO
QA[31:0]	IN	DATA OUT for Port A of FIFO
QB[31:0]	IN	DATA OUT for Port B of FIFO

5.0 SD Standard Register Map

0F-00h	SD Command Generation
1F-10h	Response
23-20h	Buffer Data Port
2F-24h	Host Controls
3D-30h	Interrupt Controls
4F-40h	Capabilities
53-50h	Force Event
5F-54h	ADMA
	Reserved
FF-F0h	Common Area

Figure 11 : SD Standard Register Map

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

The standard register map is as shown in the Figure 11. Before initializing the transaction, host driver should set all these registers sequentially. As per SD specification 2.0, registers are classified into 9 categories as shown below:

- SD Command Generation: Register to support Command Generation [0F-00h]
- Response: Register to store Response from the Device [1F-10h]
- Buffer Data Port: Registers to access Internal Data Buffer [23-20h]
- Host controls: Register to Store state of the Controller (status) [2F-24h]
- Interrupt controls: Interrupt control Register (Masks, Enable, Status) [3D-30h]
- Capabilities: Register for vendor specific capabilities of the controller [4F-40h]
- Force Event: Software Interface registers to generate events [53-50h]
- ADMA: Advance DMA Control Register [5F-54h]
- Common Area: Common Information Area (for multiple card support) [FF-F0h]

5.1 SD Host Controller Register Map

Table 5: SD Host Controller Register Map

Offset	15-08 bit	07-00 bit	Offset	15-08 bit	07-00 bit
002h	SDMA System Address (High)		000h	SDMA System Address (Low)	
006h	Block Count		004h	Block Size	
00Ah	Argument1		008h	Argument0	
00Eh	Command		00Ch	Transfer Mode	
012h	Response 1		010h	Response0	
016h	Response3		014h	Response2	
01Ah	Response5		018h	Response4	
01Eh	Response7		01Ch	Response6	
022h	Buffer Data Port1		020h	Buffer Data Port 0	
026h	Present State		024h	Present State	
02Ah	Wakeup Control	Block Gap Control	028h	Power Control	Host Control
02Eh	Software Reset	Timeout Control	02Ch	Clock Control	
032h	Error Interrupt Status		030h	Normal Interrupt Status	
036h	Error Interrupt Status Enable		034h	Normal Interrupt Status Enable	
03Ah	Error Interrupt Signal Enable		038h	Normal Interrupt Signal Enable	
03Eh			03Ch	Auto CMD12 Error Status	
042h	Capabilities		040h	Capabilities	
046h	Capabilities (Reserved)		044h	Capabilities (Reserved)	
04Ah	Maximum Current Capabilities		048h	Maximum Current Capabilities	
04Eh	Maximum Current Capabilities (Reserved)		04Ch	Maximum Current Capabilities (Reserved)	
052h	Force Event for Error Interrupt Status		050h	Force Event for Auto CMD12 Error Status	
053h			054h		
05Ah	ADMA System Address [31:16]		058h	ADMA System Address [15:00]	
05Eh	ADMA System Address r63:48)		05Ch	ADMA System Address [47:32]	
0F2h			0F0h		
FEh	Host Controller Version		0FCh	Slot Interrupt Status	

6.0 SD Protocol

Secure Digital is a synchronous serial command-response type of protocol that can do bulk data transfers using either 1-bit or 4-bit parallel data lines. In both modes, one clock line is used for synchronization and one command line for sending SD command frames. In 4-bit mode the bulk transfer throughput is four times than that of 1-bit mode. Cyclic redundancy check is used to detect errors during data transfers.

Table 6 : SD Card Interface

Name	SD Description
CD/DAT3	Card Detect/Data Line[Bit 3]
CMD	Command/Response
CLK	Clock Line
DAT0	Data Line [Bit 0]
DAT1	Data Line [Bit 1]
DAT2	Data Line [Bit 2]

Source: Technical Committee SD Association.(2007). *SD Specifications Part A2 SD Host Controller Simplified Specification Version 2.00*. Retrieved September 14, 2009 from SD website: http://www.sdcard.org/developers/tech/host_controller/simple_spec/Simplified_SD_Host_Controller_Spec.pdf

SD communication Channel consists of CMD, CLK and DAT [1/4] lines to communicate with the SD Device.

6.1 SD BUS Protocol

SD bus protocol is based on command-data-response bit streams that are initiated by a start bit and terminated by stop bit.

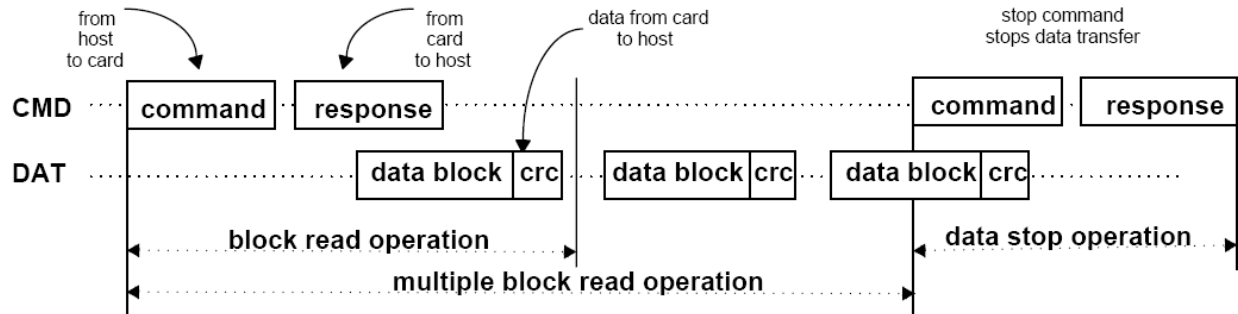


Figure 12: SD BUS Protocol

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

Command: A command Frame is a token that starts an operation which is initiated by the host, which is transmitted serially on the CMD line.

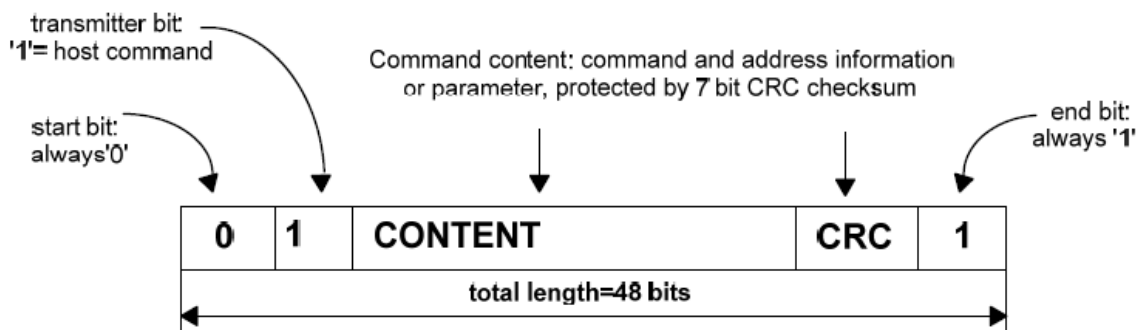


Figure 13: SD Command Frame

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

Response: A response is a token that is sent from a device to the host as an answer to a previously received command frame. Response is also transmitted serially over the CMD line.

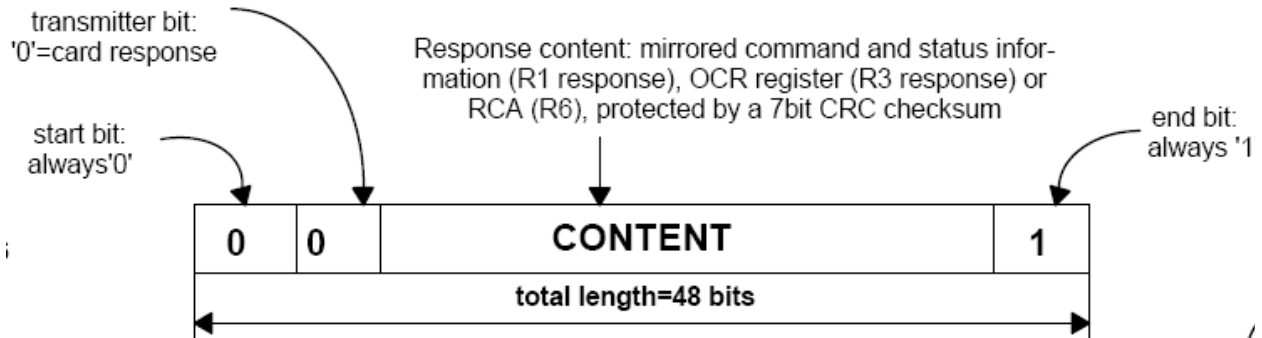


Figure 14 : Response Frame

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

Data: Data is transmitted serially on single DAT0 Line or parallel on DAT [0-3] lines between host and the device.

6.2 Data Packet Format

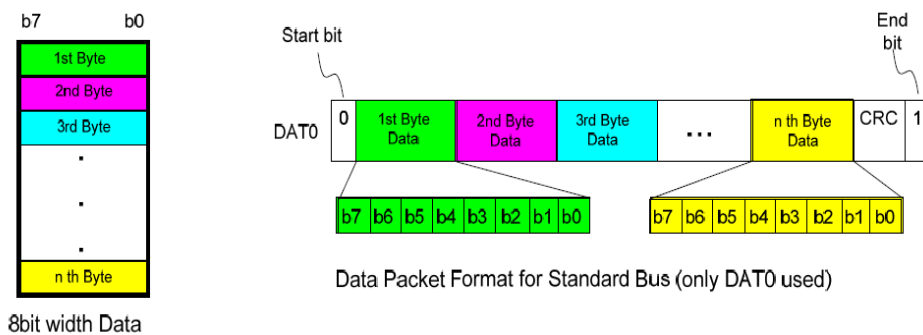


Figure 15: Data Packet Format for Standard Bus

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

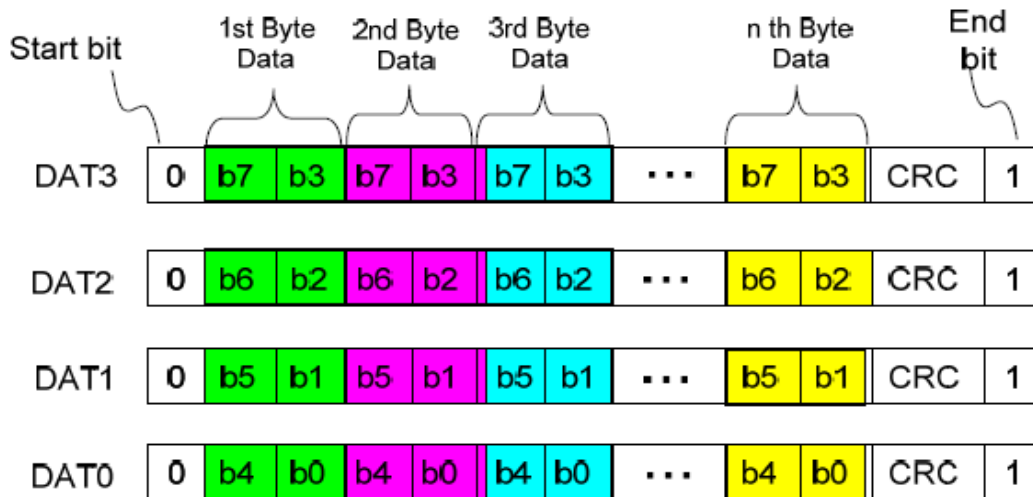


Figure 16: Data Structure in 4-bit Mode

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

6.3 SD Command Format

SD commands have a fixed code length of 48 bits as shown in figure 17. Start bit is transmitted first followed by the direction of transmission i.e for host this bit is set to '1'. The next six bits that follow transmission are command index, which is a binary coded number that can take values from 0 to 63. Some commands need arguments which are coded in to the argument bits. All SD commands are protected by CRC to detect errors during transmission.

List of SD commands are provided in the Appendix C.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	start bit	transmission bit	command index	argument	CRC7	end bit

Figure 17 : SD Command Format

Source: SanDisk Corporation. (2003). *SanDisk Secure Digital Card Product Manual Version 1.9 Document No. 80-13-0016*.

SD commands are classified into,

- Broadcast Command: Intended for all SD cards, some require Device Response.
- Address Commands: Intended for specific addressed Device to request for a Response.
- Card Identification Commands: Card Identification Commands.
- Data Transfer Commands.

Section 6.3.1 explains how and when above commands are used. Appendix C has all the details about the commands.

6.3.1 SD Card Initialization and Data Transfer

In figure 18 shows common card initialization routine and figure 19 shows SD data transfer flow.

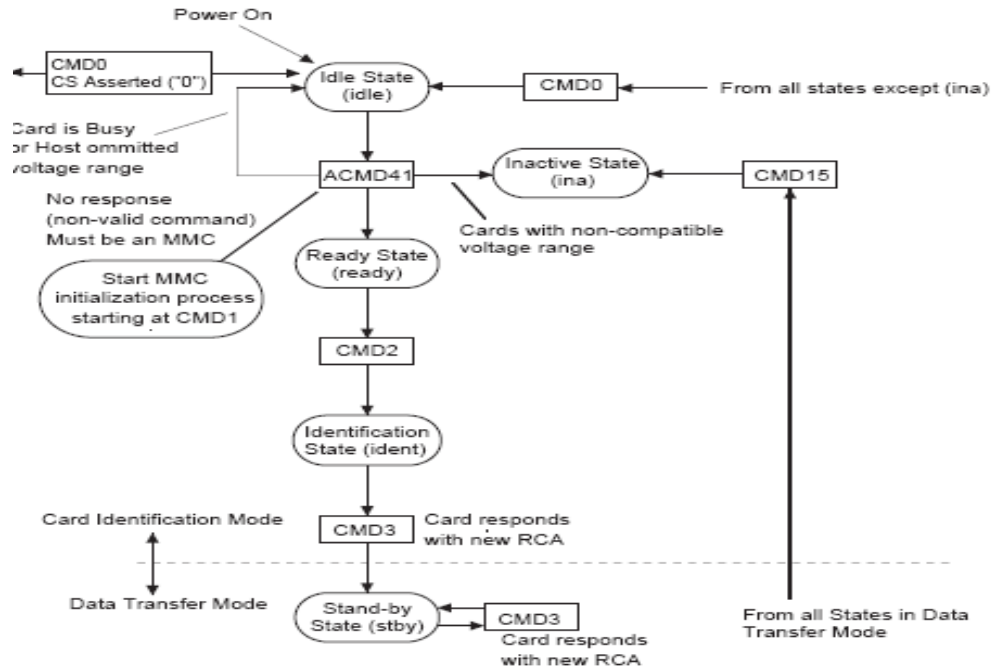


Figure 18: SD Common Initialization Routine

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

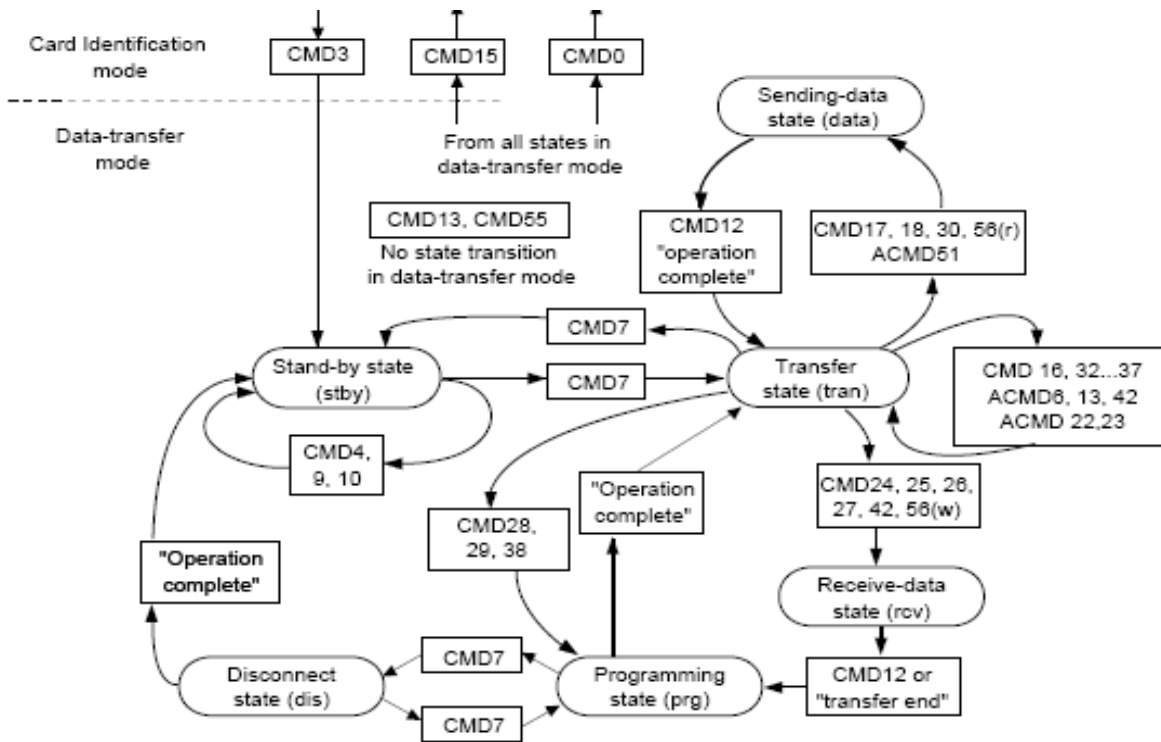


Figure 19: SD Data Transfer Flow

Source: Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf

7.0 Low Power Implementation

The major market for MS Inc., SD controller will be mobile and portable multimedia System on Chips (SoC) that runs on a battery power. To serve the above market, it is essential that the SD Controller consumes low power both under typical and absolute maximum operating conditions. Figure 20 shows a typical SoC design with an embedded microprocessor (CPU) and SD host controller.

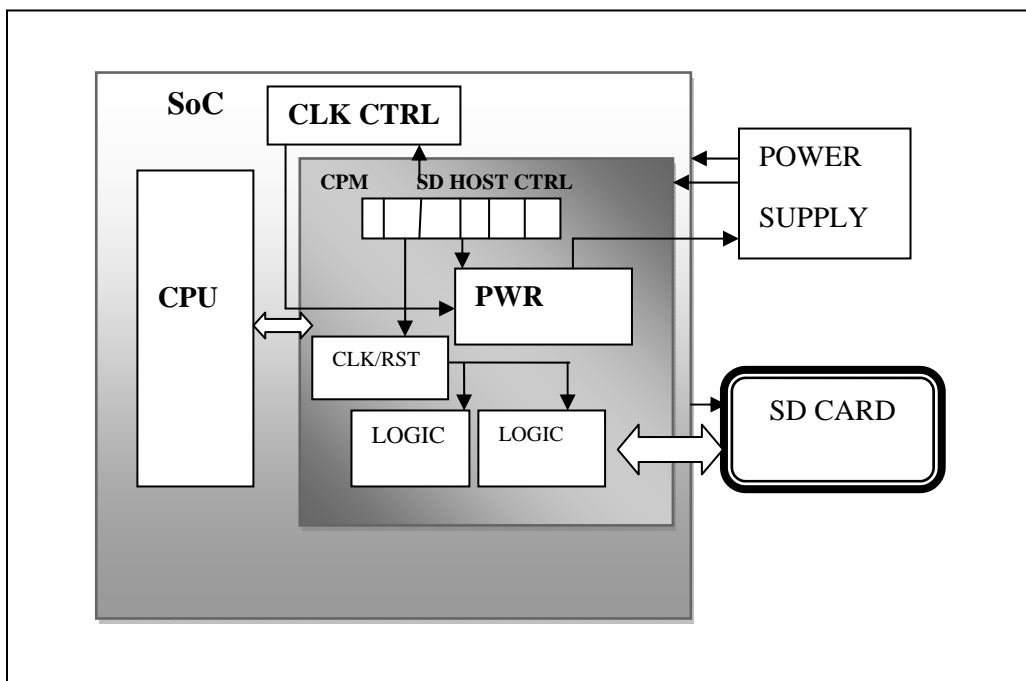


Figure 20: SoC System with SD Host Controller

7.1 Software Power management

To ensure that MS Inc.'s SD Controller IP can be used effectively in multiple applications requiring low power, the design is partitioned to support various low power techniques. A software programmable register called clock and power management (CPM) register is provided

to select the required power saving mode. The register is mapped to an address FAh of SD common register space.

CPM Register bits:

Rsvd	Rsvd	Rsvd	Fs1	Fs0	PM_en	Vs1	Vs0
------	------	------	-----	-----	-------	-----	-----

Figure 21: CPM Register

PM_en when set by the software, DMA logic and other DATA path logic will have their clock turned off during non data transfer modes. When Software programs SD Register for Data transfer these blocks become active.

Vs [1:0] can be encoded into different voltage settings. The external power regulator circuit can use these values to scale the voltage.

Fs [1:0] can be encoded into different frequency settings. These settings can be used to scale the frequency.

At the SoC level above mentioned techniques can be used to save static and dynamic power based on the Application.

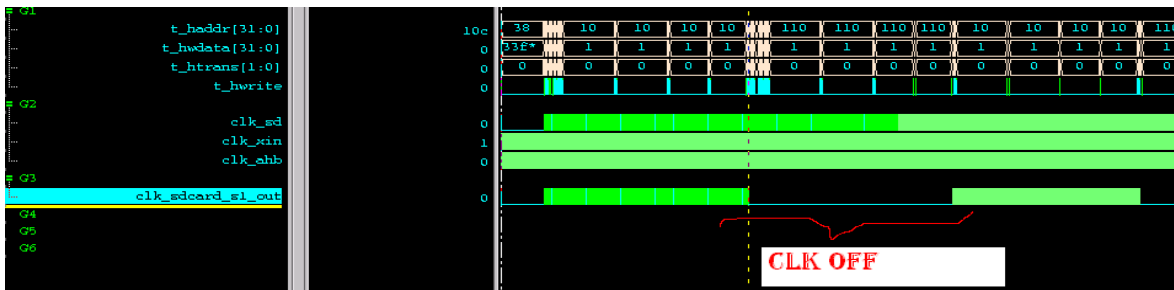


Figure 22: Simulation showing Clock cut off when there is not data transfer

7.2 Clock Gating and Voltage Scaling

In most of the digital designs the activity is synchronous to clock signal. Clock signal toggles every clock cycle switching the CMOS circuit ON and OFF resulting in significant amount of dynamic power dissipation. Therefore by gating or shutting off the clock when not need will save significant amount of dynamic power. Using low power synthesis tool, clock gating logic can be inserted into the design as shown in Figure 21.

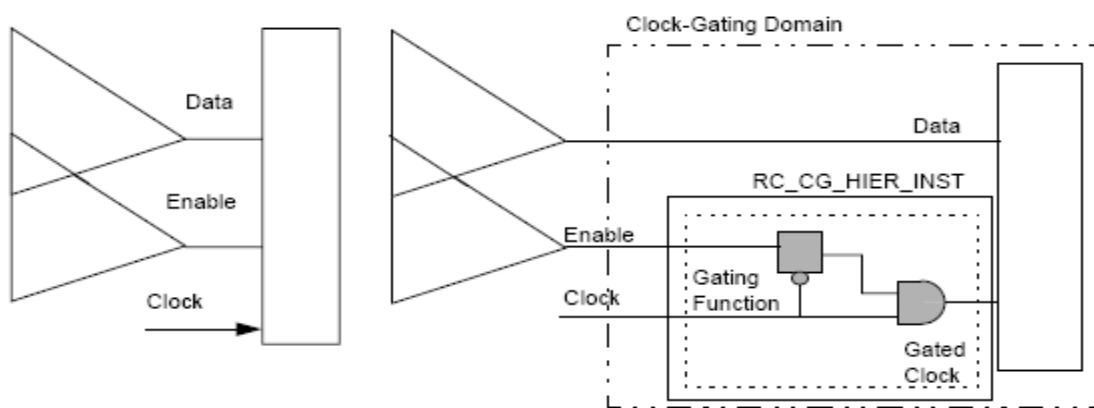


Figure 21. Clock Gating

Source: Cadence (2007). *Low Power in Encounter RTL Compiler* Retrieved on May 1, 2010. From website: http://www.ing2.unirc.it/portale/didattica/files_docenti/6131520080513113333.pdf

In order for the synthesis tool to insert clock gating circuit, tool specific RTL coding guide lines must be followed. In this project cadence RTL compiler synthesis tool is used to insert clock gating circuit. With clock gating implementation, the design area reduced by **10%** and the total power reduced by **44%**.

Quality of Report: With Clock Gating			without Clock Gating		
Category	Number	%	Category	Number	%

RC Clock Gating Instances	178	-	RC Clock Gating Instances	0	-
Non-RC Clock Gating Instances	0	-	Non-RC Clock Gating Instances	0	-

RC Gated Flip-flops	2454	64	RC Gated Flip-flops	0	0
Non-RC Gated Flip-flops	0	0	Non-RC Gated Flip-flops	0	0
Ungated Flip-flops	1380	36	Ungated Flip-flops	3834	100
Total Flip-flops	3834	100	Total Flip-flops	3834	100

Area & Power			Area & Power		

Total Area	81038.675		Total Area	89869.889	
Cell Area	33062.337		Cell Area	34992.619	
Leakage Power	0.246 mW		Leakage Power	0.269 mW	
Dynamic Power	1.208 mW		Dynamic Power	2.349 mW	
Total Power	1.455 mW		Total Power	2.618 mW	
Number of Clock Gating Logic	178				

Table 7: Dynamic Power (MW/MHz)

Core			
Vdd	0.81V	0.88V	0.99V
W/O Clock gating	2.134	2.349	3.053
W/Clock gating	1.162	1.208	1.516

Table 8: Leakage Power (MW)

Core			
Vdd	0.81V	0.88V	0.99V
W/O Clock gating	0.086	0.269	0.474
W/Clock gating	0.076	0.246	0.438

Table 9: Total Power (mW)

Core			
Vdd	0.81V	0.88V	0.99V
W/O Clock gating	2.22	2.618	3.526
W/Clock gating	1.162	1.455	1.954

7.3 Multi Vt Optimization

During synthesis, following multi Vt libraries are provided to the tool to manage timing and power.

sc9mc_cln40g_base_hvt_c50_ss_081_m40_nldm.lib

sc9mc_cln40g_base_rvt_c50_ss_081_m40_nldm.lib

Table 10: Total Power with Multi-Threshold Voltage (mW)

Core			
Vdd	0.81V	0.88V	0.99V
W/O Clock gating	2.22	2.618	3.526
W/Clock gating	1.162	1.455	1.954

There was not much of a improvement on power as the design was meeting timing.

Project Schedule – Semester II

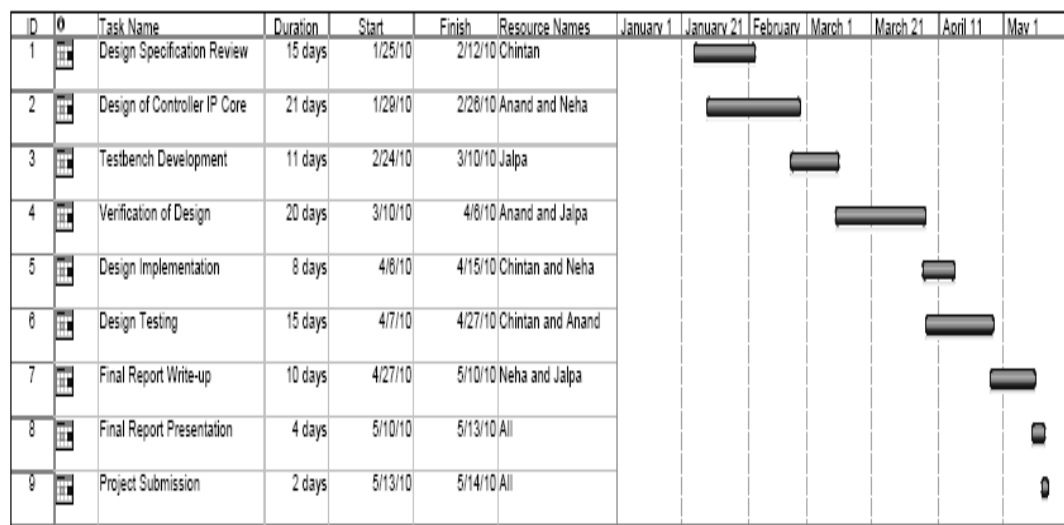


Figure 23 : Project Schedule

Table 11: Project Schedule

ID	Task Name	Duration	Start Date	End Date	Resource Name
1	Design Specification Review	15 days	1/25/2010	2/12/2010	Chintan
2	Design of Controller IP core	21 days	1/29/2010	2/26/2010	Anand and Neha
3	Testbench Development	11 days	2/24/2010	3/10/2010	Jalpa
4	Verification of Design	20 days	3/10/2010	4/6/2010	Anand and Jalpa
5	Design Implementation	8 days	4/6/2010	4/15/2010	Chintan and Neha
6	Design Testing	15 days	4/7/2010	4/27/2010	Chintan and Anand
7	Final Report Write-up	10 days	4/27/2010	5/10/2010	Neha and Jalpa
8	Final Report Presentation	4 days	5/10/2010	5/13/2010	All
9	Project Submission	2 days	5/13/2010	5/14/2010	All

8.0 Economic Justification

An Economic Justification gives an overall idea about the success of the business plan and strategies which should be taken into account to launch the product into the market once it is developed. The justification also helps to study the market of SD card. MS Inc. will provide the memory card controller with security features, which will consume less power to capture the market shares in no time. It is estimated that by the end of year 2012, 40.7 millions of units of chips will be sold by four customers and the expected profit will be \$145,400. It also covers the predicted sale in the future, profit margin and break-even point for the company.

8.1 Executive Summary

SD memory card is the most popular digital storage media used across dozens of products available in the market today. To communicate with these cards, SD host controller is required. Most of the SD memory cards are used in portable, battery operated devices. With the advent of nano technologies, the density and the operating speed of the integrated circuits inside these portable devices have increased tremendously. With more and more functionalities integrated into the same chip, the power consumption has become the limiting factor in fulfilling the market demand.

The low power SD host controller developed in this project will consume 20% less power compared to its competitors without sacrificing the performance. The low power features offered by this SD host controller in any multimedia SoC (System on Chip) chips will guarantee to maximize the battery life.

The company's main targeted customers are Mobile Smart Phones, Digital Camera and Multimedia SoC and Navigation/PC manufactures. These companies will pay initial license fee

of U.S. \$100,000 per project and little royalty of two cents for every chip sold. The funds for the initial investment will be from bank loan. We will hit break-even point by beginning of the year 2011 when four licenses will be sold. The company will make profit from license fee and the royalty there after.

MS Inc. will market the low power SD controller through SD Association (SDA) marketing events and news releases. The company will also approach potential customers through market research and demonstrate low power capabilities of their SD host controller. MS Inc. will extend their full support to their customers in integrating the low power SD controller into their design and meeting their power requirements.

8.2 Problem Statement

Battery powered portable devices like mobile phones and multimedia products are combining many features on a single chip. SD host controller is one of the designs on these chips. As the features on the devices are increasing, the demand for more power requirement is also increasing. In the absence of low power design techniques, portable devices will suffer from low battery life or need heavy battery pack. The design IP's inside SoC's need to be power efficient. The world needs low power SD controller without sacrificing performance.

8.3 Solution & Value Proposition

MS Inc.'s objective is to design SD controller using low power design technique that consumes 20% less power than the controllers available in the market, and at the same time not sacrificing the performance. In this IP, power management circuit will intelligently switch off power to the blocks that are not needed to be active during particular mode of operation. By

using clock gating and multi threshold voltage techniques appropriately, the SD host controller design will consume less power.

8.4 Market Size

Reports collected from internet, IDC and Gartner indicate that, out of all the memory storage formats used for portable devices, SD format has 56.6 % market share (PRNewswire, 2003).

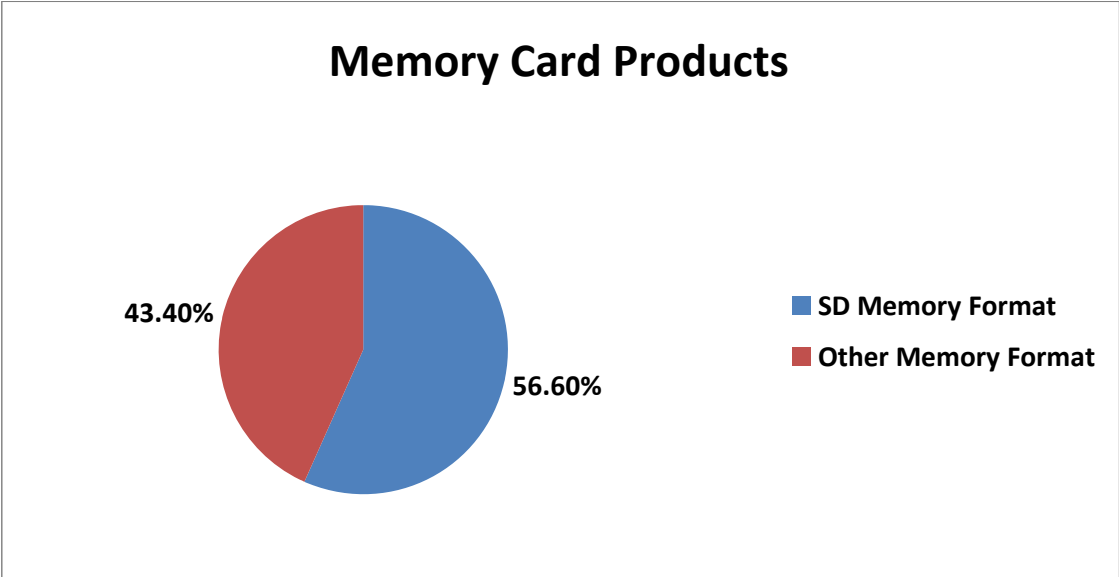


Figure 24: SD Market Size

Source: SD Association (2008). SD Technology OverviewCard: Capturing the World at the Speed of Life. Retrived from website: <http://www.sdcard.org/developers/tech>

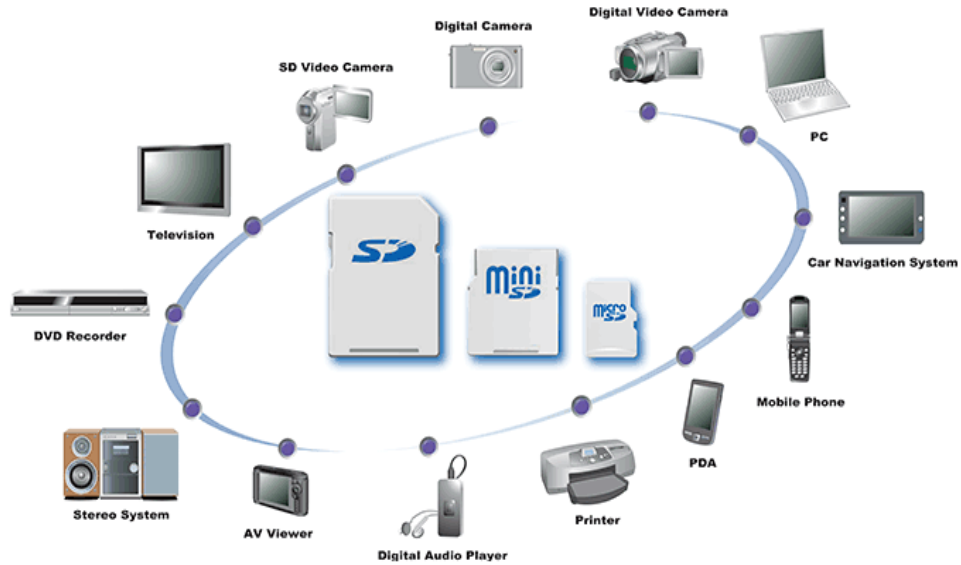


Figure 25: Products using SD format to store digital content

Source: SD Association (2008). SD Technology OverviewCard: Capturing the World at the Speed of Life. Retrived from website: <http://www.sdcard.org/developers/tech>

Report from leading Analyst's indicates that 85.6% of these smart phones will be built upon SD technology.

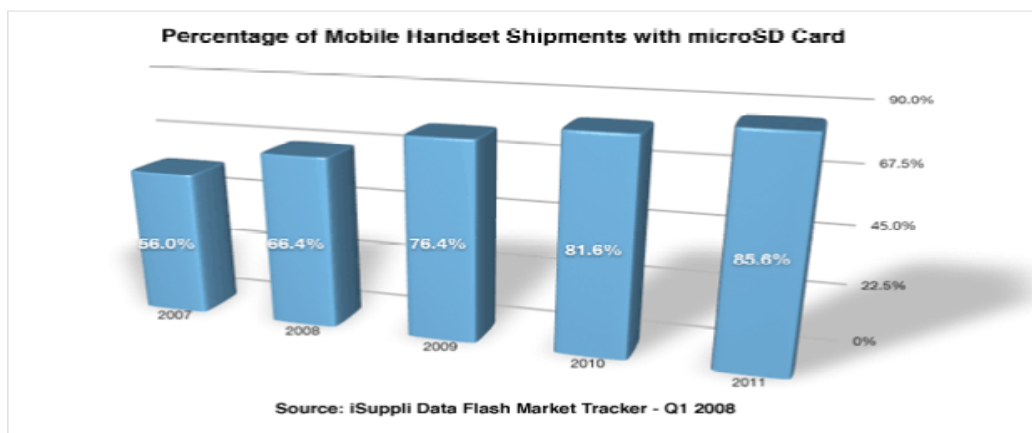


Figure 26: Mobile Phone Market with SD Cards

Source: SD Association (2008). microSD Card: Smallest Size Card Featuring the Power, Reliability and Speed of the SD Card. Retrived from website: <http://www.sdcard.org/developers/tech/microsd/>

Market Analysis show that mobile phone market generated \$4 billion in revenues in 2006 and the market is expected to generate over \$30 billion in revenues by 2012 (Pandey, 2007).

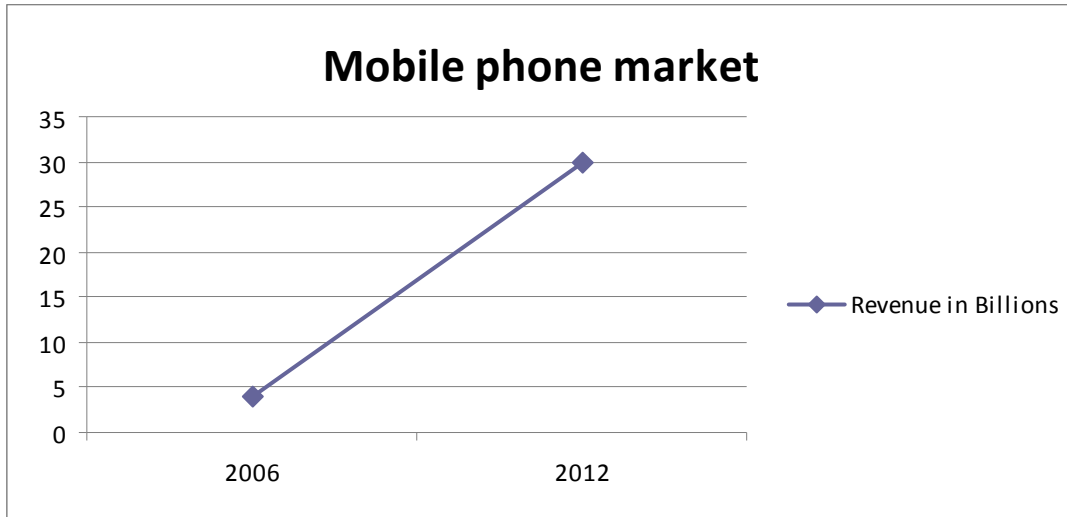


Figure 27: Mobile Phone Market

Company	2Q09 Market		2Q08 Market	
	Sales	Share (%)	Sales	Share (%)
Nokia	18,441.0	45.0	15,297.9	47.4
Research In Motion	7,678.9	18.7	5,594.2	17.3
Apple	5,434.7	13.3	892.5	2.8
HTC	2,471.0	6.0	1,330.8	4.1
Fujitsu	1,249.0	3.0	1,071.5	3.3
Others	5,688.2	13.9	8,085.8	25.1
Total	40,962.8	100.0	32,272.7	100.0

Note: For HTC, Gartner counts only the company's own-branded devices, including the G1.
Note: Totals may not add to 100.0 percent due to rounding.
Source: Gartner (August 2009)

Figure 28: Worldwide Smartphone Sales

Source: Kairer, R. (2009). Gartner Reports 2Q 2009 Mobile Phone Sales. Retrived on October 17, 2009 from PalmInfocenter website: <http://www.palminfocenter.com/news/6756/gartner-reports-2q-2009-mobile-phone-sales/>.

8.5 Competitors

Arasan Chip systems, Ricoh, Eureka, Synopsys Inc., are top most players in providing customers with SD host controller IP. Arasan Chip systems has major market share compared to others.

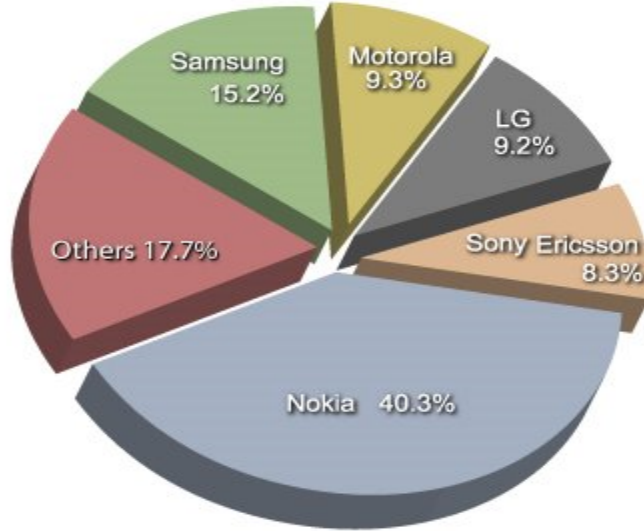
MS Inc. will use low power design techniques and process technology to consume 20% less power compared to our competitors. This will be proven to customers on a FPGA platform. The company with its experienced staff is confident about providing world class support to their customers. It will also provide assistance to the customers in integrating low power SD host controller IP in to their SOC designs.

8.6 Customers

Any Electronics Industry in need for a low power and high performance SD Host Controller IP is a customer of MS Inc. The company main targeted customers are Mobile Smart phones, Digital Camera manufactures, multimedia SOC IC developers, and Navigation/PC manufactures.

MS Inc. will target the mid size and small size companies and later will target the large scale companies like Nokia, Samsung, and Motorola etc. The Figure 29 shows the worldwide market share of the listed companies for the third quarter of year 2008.

Mobile Device Vendor Market Share, 2Q 2008



(Source: ABI Research)

Figure 29 : Mobile Device Vendor Market Share

Source: gadgetophilia.com

8.7 Cost

SD Host controller IP cost will be based upon following flexible licensing:

- Annual Licensing Fee: Customer will pay upfront license fee for whole year. By paying Annual renewal fee, customer will get maintenance and new IP's at a discounted price. In this contract, customer automatically will get upgrades to the IP when any new feature is added. Customer will not need to pay royalty for the 1st year. After that, customer needs to pay royalty of two cents on every chip he sells with the IP.
- Per Project Licensing Fee: Customer will pay upfront licensing fee per project basis. Customer will need to pay royalty of two cents on every chip he sells with the IP.

8.8 Price Point

MS Inc. being start up, it is very important to attract customers by providing competitive pricing. It is estimated that for a design of this kind requires at least four employees working 40 hrs/week for 16 weeks. For a customer it costs \$128,000 and 16 weeks lag to the market.

$$4 \text{ Engineers} \times \$50/\text{hr} \times 40 \text{ hrs/wk} \times 16\text{wk} = \$128,000$$

MS Inc. will license its low power IP design for a price of \$100K to the customer. The customers will benefit from its low power architecture and will save sixteen weeks to time to market.

8.9 Personnel

8.9.1 R&D Staff

For this project, the company has four experienced Engineers with following background:

- Mater's in Electrical Engineering
- Excellent Knowledge in Digital Design
- Good knowledge in writing Verilog code for ASIC
- Excellent understanding of Low power digital design methodology
- Good knowledge in using Synthesis tools and RTL compiler
- Good knowledge in SD protocol

8.10 SWOT

Table 12: SWOT Analysis

<p style="text-align: center;">Strength</p> <ul style="list-style-type: none"> ➤ Low power design expertise ➤ Demand for Low power SD controller ➤ Flexible Licensing features ➤ Commitment to provide Quality or Service 	<p style="text-align: center;">Weakness</p> <ul style="list-style-type: none"> ➤ Start-up company ➤ Limited budget (cannot afford High end power tools) ➤ Limited resources
<p style="text-align: center;">Opportunities</p> <ul style="list-style-type: none"> ➤ Battery operated Smart Phones & portable Multimedia SoC designs need low power IP's ➤ The report from market analysts is that 85% of Smart Phones and Multimedia devices will use SD cards due to their security features, performance and high memory capacity 	<p style="text-align: center;">Threats</p> <ul style="list-style-type: none"> ➤ Competition ➤ Change in memory storage technology

8.11 Business & Revenue Model

MS Inc. business model is based upon IP licensing and consultation fees. Customers will be charged upfront with annual or per project basis licensing fee. MS Inc. will also provide consultation for low power designs. Based on type of licensing fee, customers will also have to pay small royalty on the chips they sell. Company's revenue will be mix of licensing fee, consultation charges and the royalty from customers chip.

Marketing report show that SD memory and IO cards will dominate storage market in coming five years, the company expects huge profit from licensing fee and royalties. As awareness towards low power design is also increasing among the chip industries, the company also expects revenues from its consultation too.

8.12 Exit strategy

Planning Exit strategy is as important as starting a business. Following are the options that MS Inc. has in mind.

➤ **Sell Business**

MS Inc.'s one of the exit strategies is to sell business to other company. The parent company may not be in the same line of business. In return MS Inc. will receive cash. The Buyer will get IP technology. The Buyer will market IP and get all the revenue from license fee and royalty.

➤ **Merger**

MS Inc. will merge with big company and expand its business by using parent company's sales and marketing force. MS Inc. may not get cash but will get stocks options of the parent company. This will bring huge benefit to the MS Inc. and its employees.

➤ **Acquisition**

MS Inc. will also look into being acquired by other company. MS Inc. will approach third party who deal with such acquisition. By acquisition, the buyer will become owner of the business. MS Inc. will get cash and stocks in return.

➤ **Liquidation of Assets**

In worst case, MS Inc. will shutdown the business by laying off work force and sell out its assets.

8.13 Cash Flow Analysis

The company forecasted the license sale based on market survey. According to Gartner Reports, 40 million units of mobile phones were sold at the end of second quarter of the year 2009. Based on this report, MS Inc. will get revenue from the royalty charged per unit sold and the revenue by selling license fee. Table 14 and 15 shows the cash flow for MS Inc.

Following formulas are used to calculate the total revenue generated by the company (Daniel, L; Babcock, L C; & Morse, 2002).

Total Cost = Fixed cost + Variable Cost

Revenue from royalty = No. of unity sold * Unit royalty price

License Revenue = No. of licenses sold * Unit price of licenses

Profit/Loss = Revenue – Cost

Table 13 shows the approximate number of units sold in millions from year 2010 to 2014.

Table 13: Units sold by the Companies

Customer	Mobile Market Share %	No. of Chips Sold in 2010 (in Millions)	No. of Chips Sold in 2011 (in Millions)	No. of Chips Sold in 2012 (in Millions)	No. of Chips Sold in 2013(in Millions)	No. of Chips Sold in 2014(in Millions)
Nokia	41.2	0	10	30	50	70
Samsung	19.1	0	0	0	0.80	6
Apple	10.8	0	0	0	0.80	5
Motorola	6.2	0	0	10	0	0.75
Sony Ericsson	5.4	0	0	0	0	0.85
Fujitsu	3.8	0	0	0	0	0
Others	13.5	0	0.52	0.7	1.0	2.3

Table 14 shows approximate calculations of cash flow for MS Inc.

Table 14: Cash Flow Analysis

Year	2010	2011	2012	2013	2014
No of Customers	0	3	4	5	7
License fees charged	\$0	\$100,000	\$100,000	\$100,000	\$75,000
Revenue from Royalty	\$0	\$0	\$210,400	\$814,000	\$1,052,000
Fixed cost	\$100,000	\$100,000	\$100,000	\$100,000	\$100,000
Variable cost	\$355,000	\$355,000	\$365,000	\$490,000	\$525,000
Total cost	\$455,000	\$455,000	\$465,000	\$590,000	\$625,000
Total Revenue	\$0	\$300,000	\$610,400	\$1,314,000	\$1,577,000

Figure 30 shows the total cost and revenue generated by the company from 2011 to 2014.

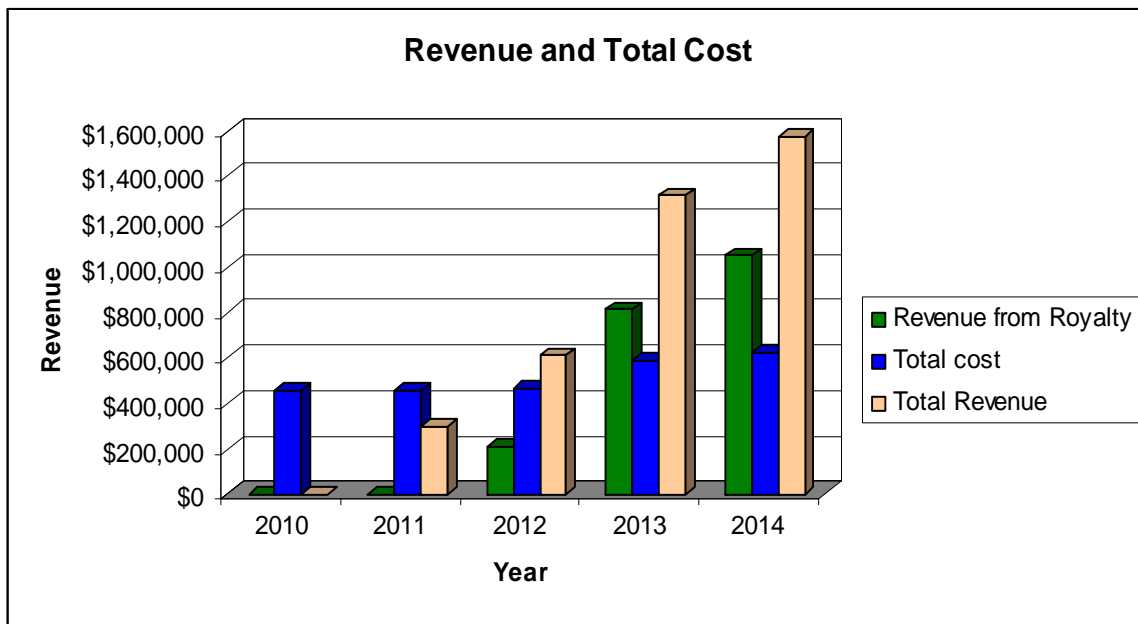


Figure 30: Revenue and Total Cost of the Company

8.13.1 Calculation of Fixed Cost

Basic operating cost of the company which includes EDA tools including licensing fee:

\$100K

8.13.2 Calculation of Variable Cost

Non Recurring cost will be as shown in Table 15.

Table 15: Calculation of Variable Cost

Year	2010	2011	2012	2013	2014
Employee Salary	\$240,000	\$240,000	\$240,000	\$300,000	\$300,000
Investment in Marketing (Advertising ,Conferences, Business travel)	\$50,000	\$50,000	\$60,000	\$100,000	\$120,000
Legal and Accounting Fees	\$30,000	\$30,000	\$30,000	\$50,000	\$50,000
System Maintenance (IT)	\$15,000	\$15,000	\$15,000	\$15,000	\$30,000
Business expenses (Office Space, Bills)	\$20,000	\$20,000	\$20,000	\$25,000	\$25,000

8.13.3 Calculation of Total Income

Table 16: Calculation of Total Income

Year	2010	2011	2012	2013	2014
No of Customers	0	3	4	5	7
License fees charged	\$0	\$100,000	\$100,000	\$100,000	\$75,000
Royalty charged	\$0	\$0	\$210,400	\$814,000	\$1,052,000
Total Revenue	\$0	\$300,000	\$610,400	\$1,314,000	\$1,577,000

9.0 Break-Even Analysis

Break-even analysis is an economic evaluation technique which is useful in relating fixed and variable costs to the number of hours of operation, the number of units produced, or other measures of operational activity. In each case, the break-even point is of primary interest in that it identifies the range of the decision variable within the most desirable economic outcome may occur. The economic success of an enterprise depends upon its ability to carry on the activities to the end that there may be a net difference between receipts and the cost of production.

(Blanchard & Farbrycky, 1990)

The linear break-even analysis is useful in evaluating the effect on profit of proposals for new operations not yet implemented and for which no data exist. The total cost including fixed and variable consists of use of facilities, material, and people. (Blanchard & Farbrycky, 1990)

The Figure 32 below shows the profitability evaluation of our project. From the graph, the break-even is in the beginning of the year 2011.

Table 17: Break Even Analysis

Year	No of customer	Fixed Cost (\$ K)	Variable Cost (\$ K)	Total Cost(\$ K)	Total Income(\$ K)	Profit (\$ K)
2010	0	100	355	455	0.0	-455.0
2011	3	100	355	455	300.0	-155.0
2012	4	100	365	465	610.4	145.4
2013	5	100	490	590	1314.0	724.0
2014	7	100	525	625	1577.0	952.0

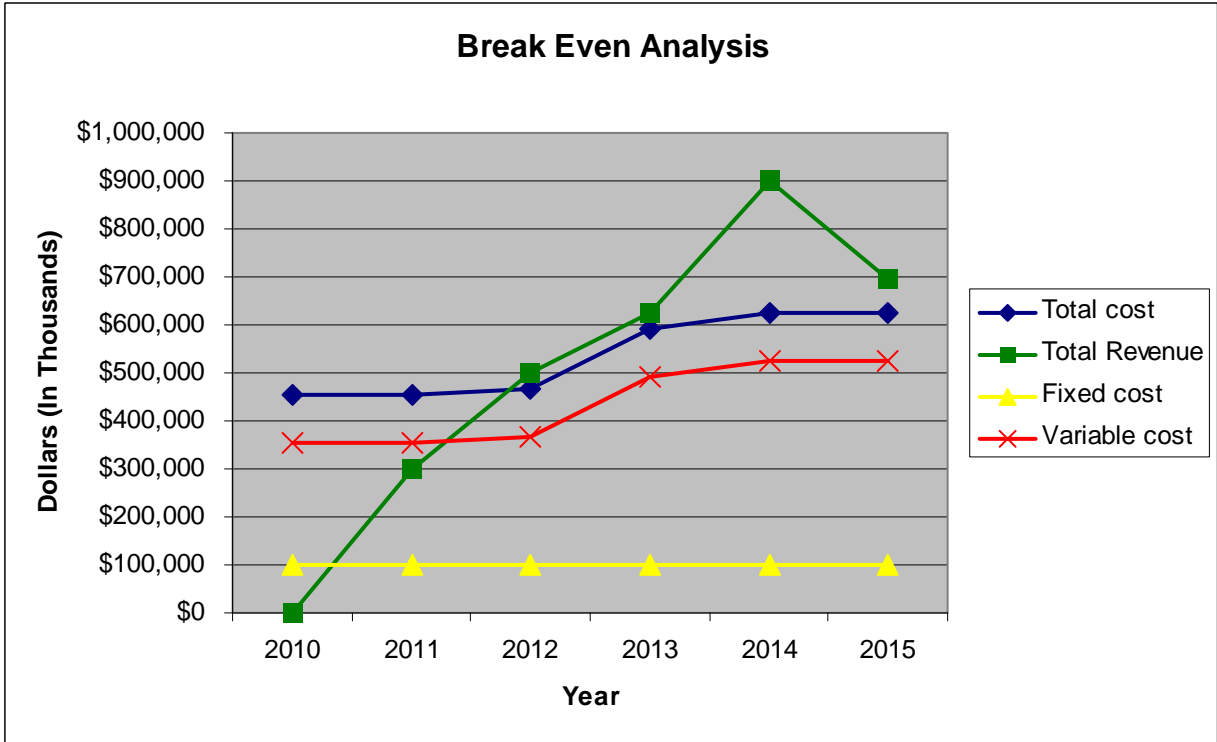


Figure 31: Break Even Analysis

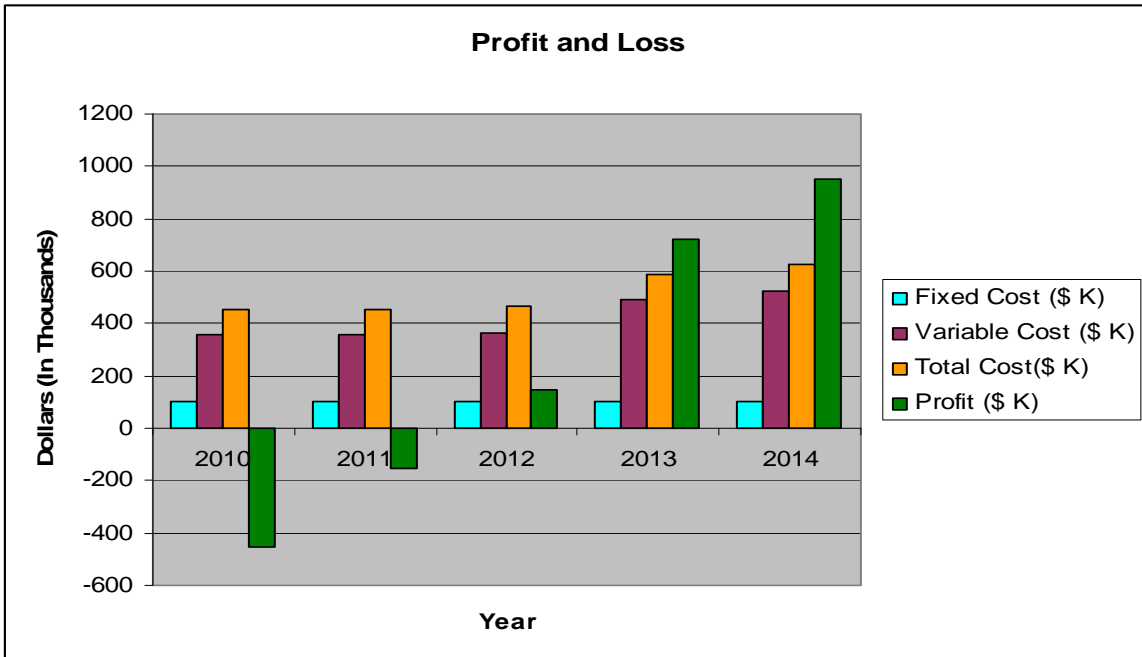


Figure 32: Profit and Loss Chart

10.0 Return on Investment (ROI)

Return on investment is a performance measure used to evaluate the efficiency of an investment or to compare the efficiency of a number of different investments. To calculate ROI, the benefit (return) of an investment is divided by the cost of the investment; the result is expressed as a percentage or a ratio.

The return on investment formula:

$$\text{ROI} = \frac{\text{Total Revenue} - \text{Cost of Investment}}{\text{Cost of Investment}}$$

Table 18 shows the simple annualized ROI calculated based on above formula.

Table 18: Calculation of ROI

Year	Total Cost (\$ K)	Total Revenue (\$ K)	ROI (Percentage)
2010	455	0.0	-100
2011	455	300.0	-34
2012	465	610.4	31
2013	590	1314.0	122
2014	625	1577.0	152

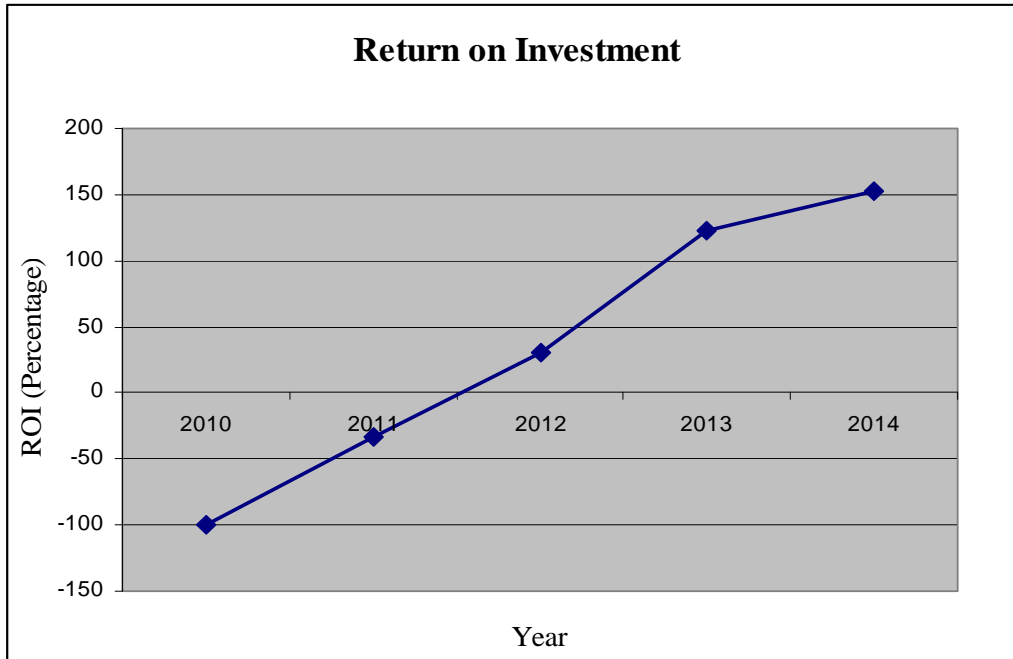


Figure 33: Return on Investment

Considering five year ROI,

$$\begin{aligned}
 &= \frac{(0 + 300 + 610 + 1314 + 1577) - (455 + 455 + 465 + 590 + 625)}{(455 + 455 + 465 + 590 + 625)} \\
 &= 46.77 \%
 \end{aligned}$$

11.0 Synthesis and Simulation Results

Simulation results are shown in Appendix A and synthesis results are shown in Appendix B.

12.0 Future Work

In coming years SD technology will be the de-facto industry standard for mobile phones, digital cameras and other portable multimedia entertainment devices. MS Inc. Future plan is to work on next generation SD which is SDXC (eXtended Capacity) memory card specification. In this technology the storage capacity of the SD card will be from 32 GB to 2 TB. The speed of the bus interface according to the specification will be in the range of 104 Mbytes to 300 Mbytes per second.

MS Inc. will also look into designing 64-bit SD host controller to communicate with 64 bit processors.

13.0 Conclusion

The battery operated device which is one of the fastest growing electronic industries, leakage power is becoming a major issue. With the proposed design of secure digital host controller intellectual property, we can achieve low power design without compromising the performance. By using clock gating and voltage scaling low power techniques, the design area reduced by 10% and the total power reduced by 44%. Results for the area and power consumption were verified by Synopsys and Cadence tools. MS Inc. will hit the breakeven in the beginning of the year 2011 and then will start making profit. Also, return on investment for the five year period is about 46%. Our product will be in the market on time to get the maximum expected profit. The overall analysis indicates sure success of the product.

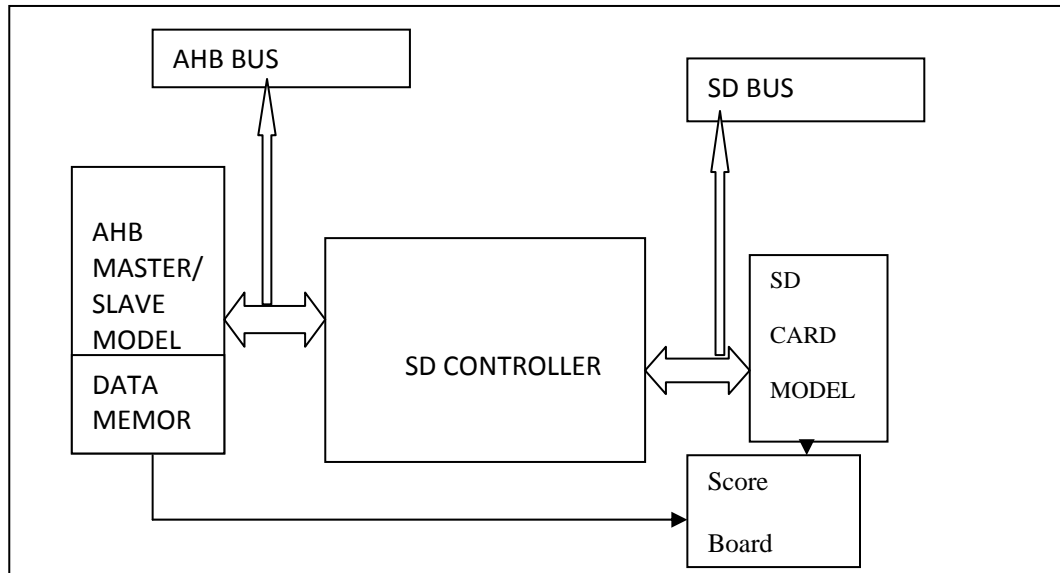
References

- Bellis M. (1997), *Inventors of the Modern Computer*. Retrieved October 1, 2009, from About.com website: <http://inventors.about.com/od/mstartinventions/a/microprocessor.ht>
- Blanchard B., and Fabrycky W., (1990). *Systems Engineering and Analysis*, Prentice-Hall, pp. 169-174.
- Donlin. M. (2008). *Low Power Is Now a High Priority*. Retrieved on September 30, 2009 from SOCCentral website: <http://www.soccentral.com/results.asp?CatID=488&EntryID=25950>
- Kneating M., Flynn D., Aitken R., Gibbons A., & Shi K. (2007). *Low power methodology manual (LPMM)*.
- Pandey, S. (2007). *UFS to Fuel Rapid Growth of the memory Card Market*. Retrieved on October 14, 2009 from website: http://www.abiresearch.com/Blog/Wireless_Blog/423
- Paring T., & Bowers H. (1996). *Literature Survey and Analysis of Low-Power Techniques for Memory and Microprocessors*. Retrieved September 16, 2009 from utexas website:http://users.ece.utexas.edu/~bevans/courses/ee382c/lectures00_welcome/project2.html
- PRNewswire (2003). *Global format dominance projected for SD memory card*. Retrieved on October 14, 2009 from website: <http://www.prnewswire.co.uk/cgi/news/release?id=109711>
- Pokhrel, K.(2007). *Physical and Silicon Measures of Low Power Clock Gating Success: An Apple to Apple Case Study*. Retrieved on September 29, 2009 from SNUG website: <http://www.snug-universal.org/cgi-bin/search/search.cgi?San+Jose,+2007>
- SanDisk Corporation.(2003). *SanDisk Secure Digital Card Product Manual Version 1.9.pdf*.
- Technical committee SD association.(2006): *SD Specifications Part 1 Physical Layer Simplified Specification Version 2.00*. Retrieved April 02, 2010 from SD website: http://www.sdcard.org/developers/tech/sdcard/pls/Simplified_Physical_Layer_Spec.pdf
- Technical Committee SD Association.(2007). *SD Specifications Part A2 SD Host Controller Simplified Specification Version 2.00*. Retrieved September 14, 2009 from SD website: http://www.sdcard.org/developers/tech/host_controller/simple_spec/Simplified_SD_Host_Controller_Spec.pdf
- White, M., & Chen Y.(2008). *Scaled CMOS Technology Reliability Users Guide*. Retrieved on October 06, 2009 from website: <http://parts.jpl.nasa.gov/docs/NEPP07/NEPP07ScaledCMOSTechnologyReliabilityUsersGuide.pdf>

Appendix A

Test Bench

The verification environment is designed to functionally verify SD host controller. The following block diagram shows different components of the test bench.



AHB Master Model is used to initialize SD controller register and setup SD command for DATA Transfer.

AHB Slave Model responds to the requests of SD controller's AHB master. The slave model has a memory which is initialized with ADMA descriptors and data to be transmitted. It also stores the received data from the SD controller.

The bus monitors are used to check for protocol violations and to display information about the traffic.

Example:

```
# Note - AHB MASTER : Command 41 initiated
# Note - AHB MASTER :***** Display Time :-->      168690
#     NOTE - SD-DEVICE : ACMD41 IS RECEIVED
#     NOTE - SD-DEVICE : R3, RESPONSE WITH CARD POWER UP STATUS BUSY HAS SENT
#     NOTE - SD-DEVICE : R3, RESPONSE FOR ACMD41 HAS SENT
# Note - AHB MASTER : Interrupt has been asserted by the HC
```

Score Board is used for data integrity check after data transmission. The expected data and the actual data are fed to the scoreboard for comparison. The test fails if there is data mis-compare or if transmitted data is not equal to the requested transfer.

Example:

```
# Note - AHB MASTER :End of file reached in master.cmd
# NO ERR DISPLAYED FROM AHB MODEL
# NO ERR DISPLAYED FROM DEVICE MODEL
# TEST PASSED
```

Test Plan

Test name: Full_mem_mem_sd4_normal

This test checks whether the SD controller can perform DMA-4bit block continuous write and read transfers.

Test name: Full_mem_mem_sd4_blk_cnt_min_mid_max

This test initiates DMA 4-bit block mode write and read transfers with minimum, medium and maximum block count.

Test name: sd_non_dma_byte_mode_test

This test initiates non dma mode read write transactions to the sd device. This test covers 1bit byte mode, 1bit to 4-bit byte mode write/read transfer

Test name: sd_non_dma_block_mode_test

This test initiates non dma mode read write transactions to the sd device. This test covers 1bit block mode, 1bit to 4-bit block mode write/read transfer.

Test name : sd_adma2_sd4_block_max_size

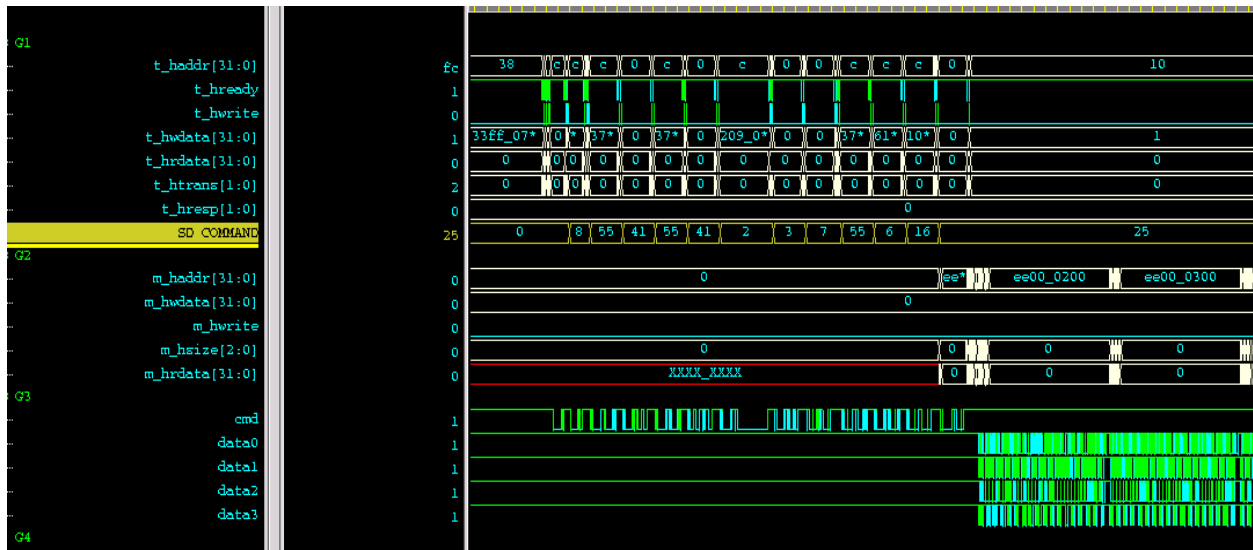
This test checks whether the sd controller can perform continuous write and read to sd card in ADMA2 4-bit mode.

Test name : sd_interrupt_test:

This test checks if sd controller can detect interrupt coming from the sd card.

Simulation Results

DMA Bulk Transfer:



Simulation Log file show various commands transmitted to read/write blocks of data:

```
# Note - AHB MASTER : Command 0 initiated
# Note - AHB MASTER :***** Display Time --> 156790
# NOTE - SD-DEVICE : CMD0 IS RECEIVED
# Note - SD DEVICE :***** Display Time --> 159020

# Note - AHB MASTER :***** Display Time --> 159750
# Note - AHB MASTER :***** Display Time --> 159870
# NOTE - SD-DEVICE : CMD8 IS RECEIVED
# Note - SD DEVICE :***** Display Time --> 162100
# Note - AHB MASTER :***** Display Time --> 163190
# Note - AHB MASTER : Command 55 initiated

# Note - AHB MASTER :***** Display Time --> 163310
# NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time --> 165540
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN IDLE STATE
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
```

```

#           NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      167820
# Note - AHB MASTER :***** Display Time :-->      168670
# Note - AHB MASTER : Command 41 initiated
# Note - AHB MASTER :***** Display Time :-->      168770
#           NOTE - SD-DEVICE : ACMD41 IS RECEIVED
# NOTE - SD-DEVICE : R3, RESPONSE WITH CARD POWER UP STATUS BUSY HAS SENT
#           NOTE - SD-DEVICE : R3, RESPONSE FOR ACMD41 HAS SENT
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command 55 initiated
# Note - AHB MASTER :***** Display Time :-->      174230
#           NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->      176460
#           NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN IDLE STATE
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT
# Note - AHB MASTER : Command 41 initiated
# Note - AHB MASTER :***** Display Time :-->      179690
#           NOTE - SD-DEVICE : ACMD41 IS RECEIVED
# NOTE - SD-DEVICE : R3, RESPONSE WITH CARD POWER UP STATUS NOT BUSY HAS SENT
#           NOTE - SD-DEVICE : R3, RESPONSE FOR ACMD41 HAS SENT
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - SD DEVICE :***** Display Time :-->      187380
#           NOTE - SD-DEVICE : R2, RESPONSE FOR CMD2 HAD SENT
# Note - SD DEVICE :***** Display Time :-->      193180
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Command 7 initiated
# Note - AHB MASTER :***** Display Time :-->      199630
#           201820SD-DEVICE : CARD IS SELECTED
#           NOTE - SD-DEVICE : CMD7 IS RECEIVED FOR SELECTION OF CARD
# Note - SD DEVICE :***** Display Time :-->      201820
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR CMD7 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      204100
# Note - AHB MASTER : Command 55 initiated
# Note - AHB MASTER :***** Display Time :-->      205530
#           NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->      207740
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      210020
# Note - AHB MASTER :***** Display Time :-->      210990
#           NOTE - SD-DEVICE : ACMD6 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->      213220
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR ACMD6 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      215500
# Note - AHB MASTER :***** Display Time :-->      216490
# OTE - SD-DEVICE : CMD16 IS RECEIVED ----->(BLOCK LENGTH) 00000100
# Note - SD DEVICE :***** Display Time :-->      218700
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR CMD16 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      220980
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : ADMA System Address register has been written
# Note - AHB MASTER :***** Display Time :-->      221910
# Note - AHB MASTER : Command 25 initiated
# Note - AHB MASTER :***** Display Time :-->      222010
#
# NOTE - AHB ARBITER: AHB BUS IS GRANTED TO THE CORE MASTER

```

```

# Note - AHB:***** Display Time -->          222090
#       222170 iface addr wr value == 04000021
# DATA LENGTH IS LOADED IN DESCRIPTOR TABLE IN SLOT
# ADDRESS IS LOADED IN DESCRIPTOR TABLE IN SLOT
# TE - SD-DEVICE : CMD25 IS RECEIVED----->(WRITE ADDRESS FOR MULTI-BLOCK) 00000000
# Note - SD DEVICE :***** Display Time -->          224220
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN RECEIVE-DATA STATE HAS SENT
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD25 HAS SENT
# Note - AHB MASTER :***** Display Time -->          227350
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE RECEIVED SUCCESSFULLY
# NOTE - SD-DEVICE : BLOCK NO IS ----->          1
# NOTE - SD-DEVICE : BYTES OF DATA RECEIVED SUCCESSFULLY -->No OF BYTE ARE      256
# Note - SD DEVICE :***** Display Time -->          250020
# NOTE - SD-DEVICE : CRC STATUS HAS SENT SUCCESSFULLY
# Note - SD DEVICE :***** Display Time -->          250300
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE RECEIVED SUCCESSFULLY
# NOTE - SD-DEVICE : BLOCK NO IS ----->          2
# NOTE - SD-DEVICE : BYTES OF DATA RECEIVED SUCCESSFULLY -->No OF BYTE ARE      256
# Note - SD DEVICE :***** Display Time -->          272060
# NOTE - SD-DEVICE : CRC STATUS HAS SENT SUCCESSFULLY
# Note - SD DEVICE :***** Display Time -->          272340
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE RECEIVED SUCCESSFULLY
#       274870 iface addr wr value == 02000021
# DATA LENGTH IS LOADED IN DESCRIPTOR TABLE IN SLOT
# ADDRESS IS LOADED IN DESCRIPTOR TABLE IN SLOT
# NOTE - SD-DEVICE : BLOCK NO IS ----->          3
# NOTE - SD-DEVICE : BYTES OF DATA RECEIVED SUCCESSFULLY -->No OF BYTE ARE      256
# Note - SD DEVICE :***** Display Time -->          294100
# NOTE - SD-DEVICE : CRC STATUS HAS SENT SUCCESSFULLY
# Note - SD DEVICE :***** Display Time -->          294380
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE RECEIVED SUCCESSFULLY
# NOTE - SD-DEVICE : BLOCK NO IS ----->          4
# NOTE - SD-DEVICE : BYTES OF DATA RECEIVED SUCCESSFULLY -->No OF BYTE ARE      256
# Note - SD DEVICE :***** Display Time -->          316140
# NOTE - SD-DEVICE : CRC STATUS HAS SENT SUCCESSFULLY
# Note - SD DEVICE :***** Display Time -->          316420
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE RECEIVED SUCCESSFULLY
#       318950 iface addr wr value == 02000023
# DATA LENGTH IS LOADED IN DESCRIPTOR TABLE IN SLOT
# ADDRESS IS LOADED IN DESCRIPTOR TABLE IN SLOT
# NOTE - SD-DEVICE : BLOCK NO IS ----->          5
# NOTE - SD-DEVICE : BYTES OF DATA RECEIVED SUCCESSFULLY -->No OF BYTE ARE      256
# Note - SD DEVICE :***** Display Time -->          338180
# NOTE - SD-DEVICE : CRC STATUS HAS SENT SUCCESSFULLY
# Note - SD DEVICE :***** Display Time -->          338460
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE RECEIVED SUCCESSFULLY
# Note - SD DEVICE :***** Display Time -->          849740
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
# NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      256
# Note - SD DEVICE :***** Display Time -->          871140
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
# NOTE - SD-DEVICE : CMD12 IS RECEIVED
# Note - SD DEVICE :***** Display Time -->          872300
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN SENDING-DATA STATE HAS SENT
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD12 HAS SENT
# Note - SD DEVICE :***** Display Time -->          874580
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time -->          874990
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Transfer complete bit set in Normal Interrupt Status Register

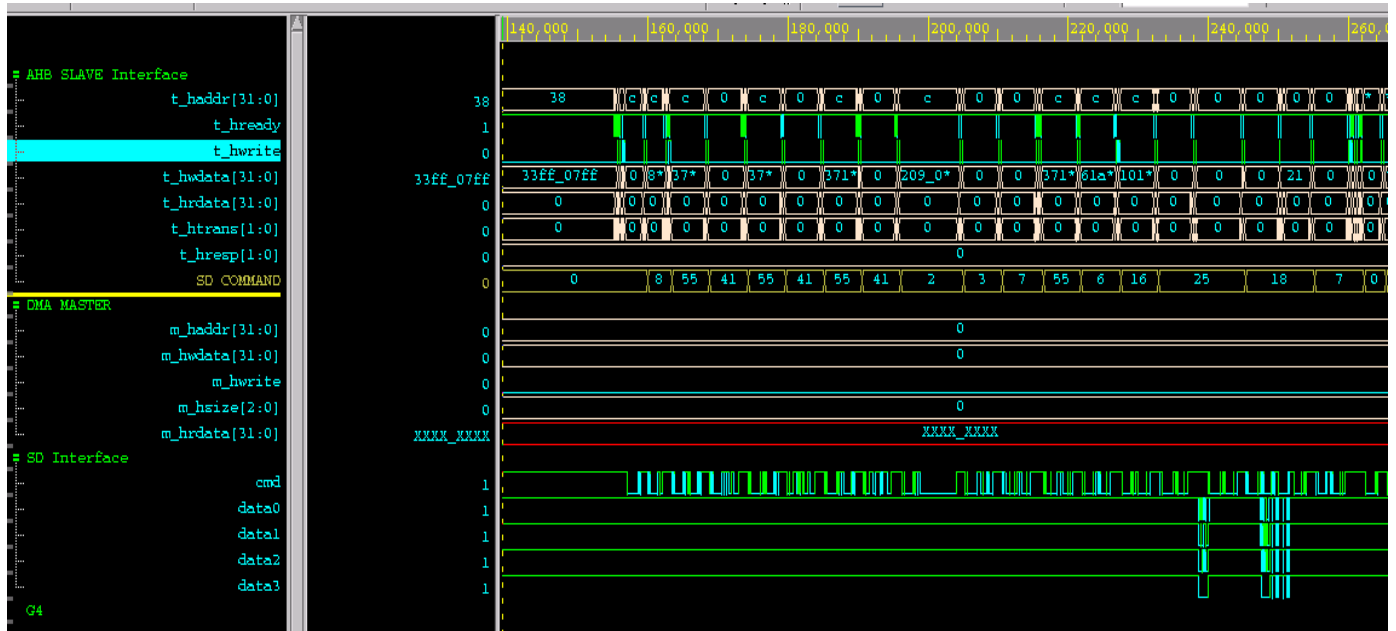
```

```

# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          875190
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER :End of file reached in master.cmd
# NO ERR DISPLAYED FROM AHB MODEL
# NO ERR DISPLAYED FROM DEVICE MODEL
# TEST PASSED

```

Non DMA Transfer:



```

Note - SD DEVICE :***** Display Time :-->          156660
# Note - AHB MASTER : Clock Control register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          156670
# Note - AHB MASTER : Command 0 initiated
# Note - AHB MASTER :***** Display Time :-->          156790
#
# NOTE - SD-DEVICE : CMD0 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          159020
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          159270
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          159470
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          159750
# Note - AHB MASTER :***** Display Time :-->          159870
# NOTE - SD-DEVICE : CMD8 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          162100

```

```

# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          162350
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          162550
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          162830
# Note - AHB MASTER : Host Controller Capabilities register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          162950
# Note - AHB MASTER : Power Control register has been written
# Note - AHB MASTER :***** Display Time :-->          163010
# Note - AHB MASTER : Power Control register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          163130
# Note - AHB MASTER : Command 55 initiated
# Note - AHB MASTER :***** Display Time :-->          163250
#
# NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          165460
#
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN IDLE STATE
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
#
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT
# Note - SD DEVICE :***** Display Time :-->          167740
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          168110
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          168310
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          168590
# Note - AHB MASTER : Command 41 initiated
# Note - AHB MASTER :***** Display Time :-->          168690
#
# NOTE - SD-DEVICE : ACMD41 IS RECEIVED
# NOTE - SD-DEVICE : R3, RESPONSE WITH CARD POWER UP STATUS BUSY HAS SENT
#
# NOTE - SD-DEVICE : R3, RESPONSE FOR ACMD41 HAS SENT
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          173550
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          173750
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          174030
# Note - AHB MASTER : Command 55 initiated
# Note - AHB MASTER :***** Display Time :-->          174150
#
# NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          176380
#
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN IDLE STATE
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
#
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT

```

```

# Note - SD DEVICE :***** Display Time :-->          178660
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          179030
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          179230
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          179510
# Note - AHB MASTER : Command 41 initiated
# Note - AHB MASTER :***** Display Time :-->          179610
#
#       NOTE - SD-DEVICE : ACMD41 IS RECEIVED
#
#       NOTE - SD-DEVICE : R3, RESPONSE WITH CARD POWER UP STATUS BUSY HAS SENT
#
#       NOTE - SD-DEVICE : R3, RESPONSE FOR ACMD41 HAS SENT
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          184470
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          184670
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          184950
# Note - AHB MASTER :***** Display Time :-->          184950
# CARD DOES NOT SUPPORT HIGH CAPACITY but VERSION 2.0
# Note - AHB MASTER : Command 55 initiated
# Note - AHB MASTER :***** Display Time :-->          185070
#
#       NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          187300
#
#       NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN IDLE STATE
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
#
#       NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT
# Note - SD DEVICE :***** Display Time :-->          189580
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          189950
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          190150
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          190430
# Note - AHB MASTER : Command 41 initiated
# Note - AHB MASTER :***** Display Time :-->          190530
#
#       NOTE - SD-DEVICE : ACMD41 IS RECEIVED
#
#       NOTE - SD-DEVICE : R3, RESPONSE WITH CARD POWER UP STATUS NOT BUSY HAS SENT
#
#       NOTE - SD-DEVICE : R3, RESPONSE FOR ACMD41 HAS SENT
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          195390
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written

```

```

# Note - AHB MASTER :***** Display Time :-->          195590
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          195870
# Note - AHB MASTER : Memory card is ready
# Note - AHB MASTER :***** Display Time :-->          195870
# CARD DOES NOT SUPPORT HIGH CAPACITY but VERSION 2.0
# Note - AHB MASTER :***** Display Time :-->          195990
#
# NOTE - SD-DEVICE : CMD2 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          198220
#
# NOTE - SD-DEVICE : R2, RESPONSE FOR CMD2 HAD SENT
# Note - SD DEVICE :***** Display Time :-->          204020
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          204390
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          204590
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
#
# NOTE - SD-DEVICE : CMD3 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          207220
#
# NOTE - SD-DEVICE : R6, RESPONSE FOR CMD3 IS HAS SENT
# Note - SD DEVICE :***** Display Time :-->          209500
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          209870
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          210070
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          210350
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          210350
# Note - AHB MASTER : RCA value is 0001
# Note - AHB MASTER :***** Display Time :-->          210350
# Note - AHB MASTER :***** Display Time :-->          210350
# Note - AHB MASTER : Command 7 initiated
# Note - AHB MASTER :***** Display Time :-->          210470
#
# 212660SD-DEVICE : CARD IS SELECTED
#
# NOTE - SD-DEVICE : CMD7 IS RECEIVED FOR SELECTION OF CARD
# Note - SD DEVICE :***** Display Time :-->          212660
#
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
#
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD7 HAS SENT
# Note - SD DEVICE :***** Display Time :-->          214940
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          215310
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Transfer complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          215510
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally

```

```

# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER : Command 55 initiated
# Note - AHB MASTER :***** Display Time :-->      216330
#           NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->      218540
#   NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      220820
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->      221190
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->      221390
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->      221670
# Note - AHB MASTER :***** Display Time :-->      221790
#           NOTE - SD-DEVICE : ACMD6 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->      224020
#   NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR ACMD6 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      226300
# OTE - SD-DEVICE : CMD16 IS RECEIVED ----->(BLOCK LENGTH) 00000008
# Note - SD DEVICE :***** Display Time :-->      229620
#   NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN TRANSFER STATE HAS SENT
#           NOTE - SD-DEVICE : R1, RESPONSE FOR CMD16 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      231900
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->      232270
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->      232470
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->      232750
# Note - AHB MASTER : Command 25 initiated
# Note - AHB MASTER :***** Display Time :-->      232870
# TE - SD-DEVICE : CMD25 IS RECEIVED----->(WRITE ADDRESS FOR MULTI-BLOCK) 00000000
# Note - SD DEVICE :***** Display Time :-->      235060
#   NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN RECEIVE-DATA STATE HAS SENT
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD25 HAS SENT
# Note - SD DEVICE :***** Display Time :-->      237340
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->      237710
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Buffer write Ready bit is set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->      237910
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally

```



```

# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          238190
# Note - AHB MASTER : 8 bytes are written to the core
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE RECEIVED SUCCESSFULLY
# NOTE - SD-DEVICE : BLOCK NO IS ----->          1
# NOTE - SD-DEVICE : BYTES OF DATA RECEIVED SUCCESSFULLY -->No OF BYTE ARE      8
# Note - SD DEVICE :***** Display Time :-->          240020
# NOTE - SD-DEVICE : CRC STATUS HAS SENT SUCCESSFULLY
# Note - SD DEVICE :***** Display Time :-->          240300
# NOTE - SD-DEVICE : CMD12 IS RECEIVED
# TE - SD-DEVICE : CMD18 IS RECEIVED----->(READ ADDRESS FOR MULTI-BLOCK) 00000000
# Note - SD DEVICE :***** Display Time :-->          247420
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
# NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      8
# Note - SD DEVICE :***** Display Time :-->          248900
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN SENDING-DATA STATE HAS SENT
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD18 HAS SENT
# Note - SD DEVICE :***** Display Time :-->          249700
# NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      8
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
# Note - AHB MASTER : Read 8 bytes from the core
# NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      8
# NOTE - SD-DEVICE : CMD12 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          251860
# NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN SENDING-DATA STATE HAS SENT
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD12 HAS SENT
# Note - AHB MASTER : Command 7 initiated
# Note - AHB MASTER :***** Display Time :-->          255070
# 257260SD-DEVICE : CARD IS DESELECTED
# Note - SD DEVICE :***** Display Time :-->          257260
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN STAND-BY STATE HAS SENT
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD7 HAS SENT
# Note - SD DEVICE :***** Display Time :-->          259540
# Note - AHB MASTER : Command 55 initiated
# Note - AHB MASTER :***** Display Time :-->          290430
# NOTE - SD-DEVICE : CMD55 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          292660
# NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN IDLE STATE
# O-DEVICE : R1, RESPONSE WITH CARD IS WAITTING FOR APP SPECIFIC COMMAND HAS SENT
# NOTE - SD-DEVICE : R1, RESPONSE FOR CMD55 HAS SENT
# Note - SD DEVICE :***** Display Time :-->          294940
# NOTE - SD-DEVICE : R3, RESPONSE WITH CARD POWER UP STATUS NOT BUSY HAS SENT
# NOTE - SD-DEVICE : R3, RESPONSE FOR ACMD41 HAS SENT
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          300750
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Command complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          300950
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Response 0 and Response 1 register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          301230
# Note - AHB MASTER : Memory card is ready

```

```

TE - SD-DEVICE : CMD18 IS RECEIVED----->(READ ADDRESS FOR MULTI-BLOCK) 00000000
# Note - SD DEVICE :***** Display Time :-->          357980
#     NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
#     NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      5
# Note - SD DEVICE :***** Display Time :-->          359220
#     NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
#     NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      5
#     NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN SENDING-DATA STATE HAS SENT
#     NOTE - SD-DEVICE : R1, RESPONSE FOR CMD18 HAS SENT
#     NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      5
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Read 5 bytes from the core
# Note - SD DEVICE :***** Display Time :-->          5885860
#     NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
#     NOTE - SD-DEVICE : BYTES OF DATA ARE SENT SUCCESSFULLY -->No OF BYTE ARE      5
# Note - SD DEVICE :***** Display Time :-->          5887180
#     NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
#     NOTE - SD-DEVICE : CMD12 IS RECEIVED
# Note - SD DEVICE :***** Display Time :-->          5887780
#     NOTE - SD-DEVICE : START BIT FOR SD 4 BIT MODE SENT SUCCESSFULLY
#     NOTE - SD-DEVICE : R1, RESPONSE WITH CARD IS IN SENDING-DATA STATE HAS SENT
#     NOTE - SD-DEVICE : R1, RESPONSE FOR CMD12 HAS SENT
# Note - SD DEVICE :***** Display Time :-->          5890060
# SD DEVICE: END OF REACHED IN DEVICE
# Note - AHB MASTER : Interrupt has been asserted by the HC
# Note - AHB MASTER : Slot Interrupt Status register is read by the Model internally
# Note - AHB MASTER :***** Display Time :-->          5890470
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER : Transfer complete bit set in Normal Interrupt Status Register
# Note - AHB MASTER : Normal Interrupt Status register has been written
# Note - AHB MASTER :***** Display Time :-->          5890670
# Note - AHB MASTER : Normal Interrupt Status register is read by the Model internally
# Note - AHB MASTER :End of file reached in master.cmd
# NO ERR DISPLAYED FROM AHB MODEL
# NO ERR DISPLAYED FROM DEVICE MODEL
# TEST PASSED

```

Appendix B

Synthesis results: Area, timing, power

Synthesis Script

```
#### Template Script for RTL->Gate-Level Flow (generated from RC v09.10-p104_1)
```

```
set_attr lp_power_unit mW /  
set_attr optimize_merge_flops false /  
set_attr optimize_merge_latches false /  
set_attr tns_opto true /
```

```
suppress_messages LBR-150  
suppress_messages LBR-147  
suppress_messages LBR-23  
suppress_messages LBR-1  
suppress_messages LBR-3  
suppress_messages LBR-40  
suppress_messages LBR-72  
suppress_messages SDC-202
```

```
lappend hdlFiles ../rtl/sdi_adma_ctrl.v  
lappend hdlFiles ../rtl/sdi_ahb_iface.v  
lappend hdlFiles ../rtl/sdi_bus_monitor.v  
lappend hdlFiles ../rtl/sdi_clock_gater.v  
lappend hdlFiles ../rtl/sdi_glitch_free_clk.v  
lappend hdlFiles ../rtl/sdi_clk_gen.v  
lappend hdlFiles ../rtl/sdi_cmd_resp.v  
lappend hdlFiles ../rtl/sdi_crc16x.v  
lappend hdlFiles ../rtl/sdi_crc7x.v  
lappend hdlFiles ../rtl/sdi_dsync.v  
lappend hdlFiles ../rtl/sdi_fifo_ctrl.v  
lappend hdlFiles ../rtl/sdi_high_ctrl.v  
lappend hdlFiles ../rtl/sdi_iface_params.v  
lappend hdlFiles ../rtl/sdi_tx_rx_ram.v  
lappend hdlFiles ../rtl/sdi_receive.v  
lappend hdlFiles ../rtl/sdi_reg_ctrl.v  
lappend hdlFiles ../rtl/sdi_reg_top.v  
lappend hdlFiles ../rtl/sdi_sync_mod.v  
lappend hdlFiles ../rtl/sdi_dft_mux.v  
lappend hdlFiles ../rtl/sdi_sync_pulse.v  
lappend hdlFiles ../rtl/sdi_synch_pulse.v  
lappend hdlFiles ../rtl/sdi_PRB08SDGZ.v  
lappend hdlFiles ../rtl/sdi_transmit.v  
lappend hdlFiles ../rtl/sdi_ram.v  
lappend hdlFiles ../rtl/sdi_wrapper.v
```

```

lappend hdlFiles ../rtl/sdi_host_top.v

#0.81V libraries
set libFilesAll
{/.automount/tsmc40g/cot/arm/arm_stdlib/sc9mc/20100302_hvt_c50_1.3.0/synopsys/lib-
nldm/sc9mc_cln40g_base_hvt_c50_ss_081_m40_nldm.lib /.a
utomount/tsmc40g/cot/arm/arm_stdlib/sc9mc/20100302_rvt_c40_1.3.0/synopsys/lib-
nldm/sc9mc_cln40g_base_rvt_c40_ss_081_m40_nldm.lib}

foreach mem $libFiles { lappend libFilesAll $mem}
set_attr library $libFilesAll /

source ./sc9mc_cln40g_base_hvt_c50_dont_use.list.tcl
foreach cell $avoidCell {
set_attr avoid true [find / -libcell $cell]
}
set lefFilesAll
{/.automount/tsmc40g/cot/arm/arm_stdlib/sc9mc/20100302_hvt_c50_1.3.0/lef/tech/1p9m_6x2z/tech.
lef /.automount/tsmc40g/cot/arm/arm_stdlib/
sc9mc/20100302_hvt_c50_1.3.0/lef/sc9mc_cln40g_base_hvt_c50.lef.antenna}
set_attr lef_library $lefFilesAll /
#set_attr cap_Table_file
/projects/svdc/mamba/users/${USER}/trunk/backend/lbr_database/cln45gs_1p09m+alrdl_6x2z_cworst.
capTable
set_attr cap_Table_file ${MB_ROOT}/mb_mem_db/cln45gs_1p09m+alrdl_6x2z_cworst.capTable

set_attr avoid true /libraries/sc9mc_cln40g_base_rvt_c40_ss_081_m40_nldm/libcells/*

### Power root attributes ###

#set_attribute lp_insert_clock_gating true /
#set_attribute hdl_track_filename_row_col true /

#####
## Load Design
#####

read_hdl -v2001 $hdlFiles
elaborate $DESIGN
puts "Runtime & Memory after 'read_hdl'"
timestat Elaboration
check_design -unresolved
#####

```

Constraints Setup

```
# Write your constraints here.
dc::create_clock clk_ahb -period 6 -waveform {0 3}
dc::set_clock_uncertainty 0.4 [ dc::get_clocks clk_ahb ]
dc::set_dont_touch_network [ dc::get_clocks clk_ahb ]
dc::create_clock clk_xin -period 20.83 -waveform {0 10.425 }
dc::set_clock_uncertainty 0.4 [ dc::get_clocks clk_xin]
dc::set_dont_touch_network [ dc::get_clocks clk_xin]
dc::create_clock -name clk_sleep_in -period 31250 -waveform {0 15625 } [dc::get_ports clk_sleep_in ]
dc::set_clock_uncertainty 0.4 [ dc::get_clocks clk_sleep_in ]
dc::set_dont_touch_network [ dc::get_clocks clk_sleep_in ]
dc::create_clock -name clk_sd -period 20.83 -waveform {0 10.425 } [ dc::get_pins u_clk_gen1/clk_sd ]
dc::set_clock_uncertainty 0.4 [ dc::get_clocks clk_sd]
dc::set_dont_touch_network [ dc::get_clocks clk_sd]
dc::create_clock -name clk_sdcard_s1_in -period 20.83 -waveform {0 10.425 } [dc::get_ports
clk_sdcard_s1_in ]
dc::create_clock -name clk_sdcard_s2_in -period 20.83 -waveform {0 10.425 } [dc::get_ports
clk_sdcard_s2_in ]
dc::set_clock_uncertainty 0.4 [ dc::get_clocks clk_sdcard_s2_in]
dc::set_dont_touch_network [ dc::get_clocks clk_sdcard_s2_in]
dc::set_dont_touch_network [ dc::get_ports rstahb_n ]
dc::set_dont_touch_network [ dc::get_pins u_reg_top1/rstahb_n ]
set ahb_inputs [ list m_hready m_hrdata m_hresp m_hgrant t_htrans t_hwrite t_hsel t_hwdata t_haddr
t_hsize t_hready_in QB ]
set ahb_outputs [ list m_hwrite m_htrans m_hsize m_haddr m_hburst m_hwdata t_hrdata t_hready
t_hresp int_to_arm m_hbusreq bus_volt_s1 bus_pow_s1 bus_vo
lt_s2 bus_pow_s2 led_on_s1 led_on_s2 AB DB CENB WENB BYTEENB]
dc::set_output_delay 2.0 -clock clk_ahb [ dc::get_ports $ahb_outputs ]
dc::set_input_delay 2.0 -clock clk_ahb [ dc::get_ports $ahb_inputs ]
set sd_inputs [ list sdcd_s1_n sdwp_s1 sdcd_s2_n sdwp_s2 cmd_in data0_in data1_in_s1 data2_in
data3_in data1_in_s2 QA ]
set sd_outputs [ list cmd_out data0_out data1_out_s1 data2_out data3_out cmd_out_en data0_out_en
data1_out_en_s1 data2_out_en data3_out_en data1_out_s2
data1_out_en_s2 AA DA CENA WENA BYTEENA]
dc::set_input_delay 14 -clock clk_sd [ dc::get_ports $sd_inputs ]
dc::set_output_delay 6 -clock clk_sd [ dc::get_ports $sd_outputs ]
dc::set_false_path -from [ dc::get_clocks clk_ahb ] -to [ dc::get_clocks [ list clk_sd clk_xin clk_sleep_in ] ]
dc::set_false_path -from [ dc::get_clocks [ list clk_sd clk_xin clk_sleep_in ] ] -to [dc::get_clocks clk_ahb]
dc::set_false_path -from [ dc::get_clocks clk_sleep_in ] -to [ dc::get_clocks [ list clk_sd clk_xin ] ]
dc::set_false_path -from [ dc::get_clocks [ list clk_sd clk_xin ] ] -to [ dc::get_clocks clk_sleep_in ]
dc::set_false_path -from [ dc::get_clocks [ list clk_sd clk_xin ] ] -to [ dc::get_clocks clk_sdcard_s1_in ]
dc::set_false_path -from [ dc::get_clocks [ list clk_sdcard_s1_in ] ] -to [ dc::get_clocks [list clk_sd
clk_xin] ]
dc::set_false_path -from [ dc::get_clocks [ list clk_sd clk_xin ] ] -to [ dc::get_clocks clk_sdcard_s2_in ]
dc::set_false_path -from [ dc::get_clocks [ list clk_sdcard_s2_in ] ] -to [ dc::get_clocks [list clk_sd
clk_xin] ]
### Latch Borrow to 0 #####
```

```

set_attr latch_borrow 0 /des*//*

if {[length [find / -subdesign *sms_wrapper]] > 0} {
set_attr preserve map_size_ok [find / -subdesign *sms_wrapper]
}

if ![file exists ${_LOG_PATH}] {
file mkdir ${_LOG_PATH}
puts "Creating directory ${_LOG_PATH}"
}

if ![file exists ${_OUTPUTS_PATH}] {
file mkdir ${_OUTPUTS_PATH}
puts "Creating directory ${_OUTPUTS_PATH}"
}

if ![file exists ${_REPORTS_PATH}] {
file mkdir ${_REPORTS_PATH}
puts "Creating directory ${_REPORTS_PATH}"
}

#####
## Preserve cells/modules ...
#####
if {{} != [set insts [find $DESIGN -instance *dOnt_*]]} {
set_attr preserve true $insts
unset insts
}

#####
## Define cost groups (clock-clock, clock-output, input-clock, input-output)
#####

if {[length [all::all_seqs]] > 0} {
define_cost_group -name I2C -design $DESIGN
define_cost_group -name C2O -design $DESIGN
define_cost_group -name C2C -design $DESIGN
path_group -from [all::all_seqs] -to [all::all_seqs] -group C2C -name C2C
path_group -from [all::all_seqs] -to [all::all_outs] -group C2O -name C2O
path_group -from [all::all_inps] -to [all::all_seqs] -group I2C -name I2C
}
define_cost_group -name I2O -design $DESIGN
path_group -from [all::all_inps] -to [all::all_outs] -group I2O -name I2O

```

```
check_design -multidrivem
#####
#####
## Synthesizing to generic
#####
#####
```

```
synthesize -to_generic -eff $SYN_EFF
puts "Runtime & Memory after 'synthesize -to_generic'"
timestat GENERIC
```

```
#####
#####
## Synthesizing to gates
#####
#####
```

```
synthesize -to_mapped -eff $MAP_EFF -no_incr
puts "Runtime & Memory after 'synthesize -to_map -no_incr'"
timestat MAPPED
#report datapath > $_REPORTS_PATH/${DESIGN}_datapath_map.rpt
```

```
#####
#####
## Incremental Synthesis
#####
#####
synthesize -to_mapped -eff $MAP_EFF -incr
puts "Runtime & Memory after incremental synthesis"
timestat INCREMENTAL
```

```
#####
#####
## Incremental Synthesis
#####
#####
```

```
## An effort of low was selected to minimize runtime of incremental opto.
## If your timing is not met, rerun incremental opto with a different effort level
synthesize -to_mapped -eff low -incr
puts "Runtime & Memory after incremental synthesis"
timestat INCREMENTAL_POST_SCAN_CHAINS
```

```
#####
#####
## write Encounter file set (verilog, SDC, config, etc.)
#####
#####
report timing -lint
report timing -lint -verbose > $_REPORTS_PATH/${DESIGN}_timing_lint.rpt

report clock_gating > $_REPORTS_PATH/${DESIGN}_clockgating.rpt
report power -depth 0 > $_REPORTS_PATH/${DESIGN}_power.rpt
report area > $_REPORTS_PATH/${DESIGN}_area.rpt
report timing -endpoints -worst 1 -slack_limit 0 > $_REPORTS_PATH/${DESIGN}_all_vio.rep
report_timing -full -worst 1 -num_path 50 -cost_group C2C >
$_REPORTS_PATH/${DESIGN}_maxpath50.rep
report_timing -full -worst 1 -num_path 50 -cost_group I2C >>
$_REPORTS_PATH/${DESIGN}_maxpath50.rep
report_timing -full -worst 1 -num_path 50 -cost_group I2O >>
$_REPORTS_PATH/${DESIGN}_maxpath50.rep
report_timing -full -worst 1 -num_path 50 -cost_group C2O >>
$_REPORTS_PATH/${DESIGN}_maxpath50.rep

report gates > $_REPORTS_PATH/${DESIGN}_gates.rep
report qor > $_REPORTS_PATH/${DESIGN}_qor.rep

set_attr ui_respects_preserve false
change_names -prefix ${DESIGN}_ -subdesign
change_names -instance -net -restricted {} -replace_str "_"
change_names -instance -net -restricted {} -replace_str NULL

write_design -basename ${_OUTPUTS_PATH}/${DESIGN}
write_sdc > ${_OUTPUTS_PATH}/${DESIGN}.sdc
```

Synthesis Results:

Clock gating Reports:

```
Operating conditions: PVT_ss_081_m40
Interconnect mode:   global
Area mode:           physical library
```

=====

Summary

```
-----
Category      Number %
```

RC Clock Gating Instances 178 -
Non-RC Clock Gating Instances 0 -

RC Gated Flip-flops 2454 64
Non-RC Gated Flip-flops 0 0
Ungated Flip-flops 1380 36
Total Flip-flops 3834 100

....

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Appendix C

SD card commands and description are appended in this section which is taken from Sandisk Manual.

SD Card Command Classes

	0	1	2	3	4	5	6	7	8	9-11
Supported Commands	Basic	Reserved	Block Read	Reserved	Block Write	Erase	Write Protection	Lock Card	Application Specific	Reserved
CMD0	+									
CMD2	+									
CMD3	+									
CMD4	+									
CMD7	+									
CMD9	+									
CMD10	+									
CMD12	+									
CMD13	+									
CMD15	+									
CMD16			+		+					
CMD17			+							
CMD18			+							
CMD24					+					
CMD25					+					
CMD27					+					
CMD28							+			
CMD29							+			
CMD30							+			
CMD32						+				
CMD33						+				
CMD38						+				
CMD42								+		
CMD55									+	
CMD56									+	
ACMD6									+	
ACMD13									+	
ACMD22									+	
ACMD23									+	
ACMD41									+	
ACMD42									+	
ACMD51									+	

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Basic Command Description

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD0	bc	[31:0] don't care*	-	GO_IDLE_STATE	Resets all cards to Idle State.
CMD1	Reserved				
CMD2	bcr	[31:0] don't care*	R2	ALL_SEND_CID	Asks any card to send their CID numbers on the CMD line. (Any card that is connected to the host will respond.)
CMD3	bcr	[31:0] don't care*	R6	SEND_RELATIVE_ADDR	Asks the card to publish a new relative address (RCA).
CMD4 ¹	Not Supported				
CMD5	Reserved				
CMD6	Reserved				
CMD7	ac	[31:16] RCA [15:0] don't care*	R1 (only from the selected card)	SELECT/DESELECT_CARD	Command toggles a card between the Stand-by and Transfer states or between the Programming and Disconnect state. In both cases the card is selected by its own relative address and deselected by any other address; address 0 deselected all. When the RCA equals 0, the host may do one of the following: —use other RCA number to perform card de-selection or —re-send CMD3 to change its RCA number to other than 0 and then use CMD7 with RCA=0 for card de-selection.
CMD8	Reserved				
CMD9	ac	[31:16] RCA [15:0] don't care*	R2	SEND_CSD	Addressed card sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] don't care*	R2	SEND_CID	Addressed card sends its card identification (CID) on the CMD line.
CMD11	adtc	[31:0] data address ²	R1	READ_DAT_UNTIL_STOP	Reads data stream from the card, starting at the given address, until a STOP_TRANSMISSION follows.
CMD12	ac	[31:0] don't care*	R1k ³	STOP_TRANSMISSION	Terminates a multiple block read/write operation.
CMD13	ac	[31:16] RCA [15:0] don't care*	R1	SEND_STATUS	Addressed card sends its status register.
CMD14	Reserved				
CMD15	ac	[31:16] RCA [15:0] don't care*	-	GO_INACTIVE_STATE	Sets the card to inactive state.

* The bit places must be filled but the value is irrelevant.

Block Read Commands

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	Selects a block length (in bytes) for all following block commands (read and write). ¹
CMD17	adtc	[31:0] data address	R1	READ_SINGLE_BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command. ²
CMD18	adtc	[31:0] data address	R1	READ_MULTIPLE_BLOCK	Continuously send blocks of data until interrupted by a stop transmission command.
CMD19 – CMD23	Reserved				

Block Write Commands

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD24	adtc	[31:0] data address	R1	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command. ³
CMD25	adtc	[31:0] data address	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows.
CMD26	Not Applicable				
CMD27	adtc	[31:0] don't care*	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.

* The bit places must be filled but the value is irrelevant.

Write Protection Commands

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD28*	ac	[31:0] data address	R1b	SET_WRITE_PROT	This command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE).
CMD29*	ac	[31:0] data address	R1b	CLR_WRITE_PROT	This command clears the write protection bit of the addressed group.
CMD30*	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	This command asks the card to send the status of the write protection bits.
CMD31	Reserved				

Error Commands

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD32	ac	[31:0] data address	R1	ERASE_WR_BLK_START	Sets the address of the first write block to be erased.
CMD33	ac	[31:0] data address	R1	ERASE_WR_BLK_END	Sets the address of the last write block of the continuous range to be erased.
CMD34 ... CMD37	Reserved				
CMD38	ac	[31:0] don't care*	R1b	ERASE	Erases all previously selected write blocks.
CMD39 ... CMD41	Reserved				

* The bit places must be filled but the value is irrelevant.

Lock Card Commands

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD42 ... CMD54	SDA Optional Commands, currently supported by SanDisk SD Card.				

Application Specific Commands

CMD INDEX	Type	Argument	Resp.	Abbreviation	Command Description
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the card that the next command is an application specific command rather than a standard command
CMD56	adtc	[31:1] stuff bits. [0]: RD/ WR ¹	R1	GEN_CMD	Used either to transfer a data block to the card or to get a data block from the card for general purpose / application specific commands. The size of the data block shall be set by the SET_BLOCK_LEN command.
CMD57 ... CMD59	Reserved				
CMD60 -63	Reserved for Manufacturer				

Application Specific Command Used/ Reserved by SD Card

ACMD INDEX	Type	Argument	Resp.	Abbreviation	Command Description
ACMD6	ac	[31:2] stuff bits [1:0]bus width	R1	SET_BUS_WIDTH	Defines the data bus width ('00'=1bit or '10'=4 bits bus) to be used for data transfer.
ACMD13	adtc	[31:0] stuff bits	R1	SD_STATUS	Send the SD Card status. The status fields are given in Table 4-28.
ACMD17	Reserved				
ACMD18	--	--	--	--	Reserved for SD security applications. ¹
ACMD19 to ACMD21	Reserved				
ACMD22	adtc	[31:0] stuff bits	R1	SEND_NUM_WR_BLOCKS	Send the number of the written (without errors) write blocks. Responds with 32bit+CRC data block.
ACMD23	ac	[31:23] stuff bits [22:0]Number of blocks	R1	SET_WR_BLK_ERASE_COUNT	Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR command). "1"=default (one wr block) ² .
ACMD24	Reserved				
ACMD25	--	--	--	--	Reserved for SD security applications. ¹
ACMD26	--	--	--	--	Reserved for SD security applications. ¹
ACMD38	--	--	--	--	Reserved for SD security applications. ¹
ACMD39 to ACMD40	Reserved				
ACMD41	bor	[31:0]OCR without busy	R3	SD_APP_OP_COND	Asks the accessed card to send its operating condition register (OCR) content in the response on the CMD line.
ACMD42	ac	[31:1] stuff bits [0]set_cd	R1	SET_CLR_CARD_DETECT	Connect[1]/Disconnect[0] the 50KOhm pull-up resistor on CD/DAT3 (pin 1) of the card. The pull-up may be used for card detection.
ACMD43 ACMD49	--	--	--	--	Reserved for SD security applications. ¹
ACMD51	adtc	[31:0] stuff bits	R1	SEND_SCR	Reads the SD Configuration Register (SCR).

NOTES: 1) Refer to *SD Card Security Specification* for detailed explanation about the SD Security Features

2) Command STOP_TRAN (CMD12) shall be used to stop the transmission in Write Multiple Block whether the pre-erase (ACMD23) feature is used or not.