High Speed Embedded Control 32-bit Microprocessor

A Project Report

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In Partial Fulfillment

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Master of Science in Engineering

By

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November 2011
The undersigned Project Committee approves the Master’s Project titled

**High Speed Embedded Control 32-bit Microprocessor**

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Approved for the Department of General Engineering

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ABSTRACT

High Speed Embedded Control 32-bit Microprocessor
by Bhavesh Patel, Himali Mistry, Sedigheh Jafarinejad, Sunita Sreepada

The fast paced market demand growth for handheld digital devices, such as smartphones and tablet devices, is urging the manufacturers to look for better technical solutions to satisfy one or more of the customers’ requirements in terms of speed, performance, power, and price. The 32-bit embedded control microprocessor is the key component of most of the current handheld digital devices. A single microprocessor design cannot satisfy the demands for high speed, high performance, low power, and low price in the same device. Therefore, the design engineers are after the designs that meet one of the customers’ requirements. The goal of this project is to introduce a design for 32-bit embedded control microprocessor that performs the functions with speeds higher than 1 GHz, with higher performance, and comparable price to the designs that are currently in the market. Each block of the design is implemented and tested to meet the high performance and high speed. The integrated design is also tested to verify the functionality at speeds higher than 1 GHz. In addition, the results of the economic analysis justify that the investment on this novel design, which is going to be introduced with a comparable price, is going to be considerably profitable and will yield a high percent return of investment in less than five years.
ACKNOWLEDGMENTS

We would like to express our utmost gratitude to Prof. Morris Jones, Part-Time Faculty, Dept. of Electrical Engineering, San Jose State University, for his support, assistance, and guidance in successfully completing this project.

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1. Introduction

During recent decades, microprocessors have been the key component used in almost all kinds of digital devices, from the smallest embedded systems and handheld devices, to the largest supercomputers.

The microprocessor is a silicon chip that controls the logic of the digital devices. It contains a Central Processing Unit (CPU), which is connected to memory and Input/Output (I/O) by buses that carry information between the units. The CPU itself contains an Arithmetic Logic Unit (ALU) and a control unit. The arithmetic operations take place in ALU. The control unit sends the signals to ALU that determine which operation should be performed at any moment (Webopedia, 2011).

Microprocessors are differentiated based on their instruction set (the set of instructions that can be executed), bandwidth (the number of bits that can be processed in each instruction), and clock speed (the number of instructions that can be processed per second). Microprocessors with higher number of bits and higher clock speed have more powerful CPUs. Microprocessors are also classified into two categories: Reduced Instruction Set Computer (RISC) and Complex Instruction Set Computer (CISC). Compared to CISC processors, RISC microprocessors execute a relatively limited number of simple instructions and require fewer of transistors. Therefore, RISC processors are very fast and cheap for design and production (Webopedia, 2011).

In the current digital world, the 32-bit embedded microprocessor covers a wide market in newer generation handheld devices and networking solutions. The expected use of smart phones in emerging countries is the vital factor driving the 32-bit embedded microprocessor market. The number of smart phone users is going to cross 1.7 billion by 2014 due to the emerging Asian market, which includes the major growing market in China and India along with surging demand in central and Latin America (Research and Markets, 2010). Net books have been replaced with the mobile computing devices that are another driving factor in worldwide processor market. Mobile computing is already changing the microprocessor industry. The number of smart phones shipped globally is expected to hit 300 million by 2012 (Research and Markets, 2010). The market trend and demand is toward designing 32-bit embedded microprocessors with the highest number of optimized characteristics (i.e. speed, performance, power, and price) that can handle...
larger software applications. However, the existing 32-bit embedded microprocessors do not meet the market demands in terms of speed, performance, and price. The existing designs do not simultaneously satisfy the demands for high speed, high performance, and reasonable price.

To meet the market and customers’ demands, four engineers from San Jose State University are establishing a company named “Quad Logic” to work on the project of designing a high speed 32-bit embedded control microprocessor with focus on speeds over 1 GHz and high performance compared to the similar existing products, but with comparable price. The design, which is going to be introduced by Quad Logic, will satisfy the customers’ demand for high performance by using the pipeline approach. This approach would also allow the microprocessor to execute the instructions with speeds higher than 1 GHz. The design is implemented by using the latest technology available in the market for its transistor’s size, which is 45nm technology, to achieve the desired performance and speed. Based on results of the market and economic analysis, the price of the final design is going to be comparable to the price of the existing designs.

2. Project Scope
To define the scope of the project, the engineers of Quad Logic searched for the current problem that the customers’ and manufacturers’ of the 32-bit embedded microprocessors are facing in terms of speed, performance, power, and price. The result was defining a project on designing a high speed 32-bit embedded control microprocessor.

Quad Logic followed a defined procedure for the design process of its product and used CAD tools for designing and testing the product. It has also planned to introduce its product by the second quarter of 2012.

2.1 Hypothesis
Design a high speed embedded control 32-bit microprocessor by targeting speeds over 1 GHz. The goal of the design is to achieve higher performance with a comparable price to similar products in the market.
2.2 Method of Investigation

For turning the hypothesis into reality and achieving the goal of the project, Quad Logic has defined a procedure for its design process and has determined the type of tools that are going to be used for design and testing of the product. It has also predicted the time periods needed for accomplishing each phase of the project and the final date that the product is going to be introduced.

2.2.1 Experimental Procedure

The following design process flow chart (Figure 1) shows the experimental procedure for our IP development. The design of 32-bit embedded microprocessor IP comprises multiple blocks. Quad Logic has designed and tested each block of the design using Spectre Simulation. It has integrated all the blocks and also tested the integrated design for the required functionality and performance.
2.2.2 Resources Utilized

Quad Logic implemented its design using CAD tools. It used Cadence Virtuoso tool for circuit design. The cadence tool has Spectre simulation facility for testing and analysis. The tools used for this project are listed below.

- Cadence “Virtuso” IC design tool for circuit design
- Jdsize calculator for transistor sizing
• Calculus softer for transistor modeling
• Spectre simulator and Verilog-A codes for testing of the design and analysis

2.2.3 Project Schedule
To achieve the objectives of this project on time, Quad Logic followed the schedule given in the Gantt chart (Appendix B).

2.3 Team and Committee Structure
Four engineering students from San Jose State University have designed the 32-bit embedded control microprocessor with the support and guidance from their academic and industrial advisers.

2.3.1 Team members

2.3.1.1 Sunita Sreepada
She is pursuing masters in general engineering with special concentration in VLSI design. She has completed ASIC CMOS design, advanced logic design, and SoC design and verification with System Verilog courses.

2.3.1.2 Sedigheh Jafarinejad
She is pursuing masters in general engineering with emphasis on electronic materials and devices. She has completed High Speed CMOS Circuits, ASIC CMOS design, and advanced logic design courses.

2.3.1.3 Himali Mistry
She is pursuing masters in electronic material and devices. She has completed ASIC CMOS design, High Speed CMOS Circuits and Advance logic design courses.

2.3.1.4 Bhavesh Patel
He is pursuing masters in general engineering with emphasis on electronic materials and devices. He has completed High Speed CMOS Circuits, ASIC CMOS design and Advanced logic design courses.
2.3.2 Committee Members

2.3.2.1 Faculty reader: Prof. Morris Jones

**Background:** Prof. Morris Jones is working as a part-time faculty in Electrical engineering department at San Jose State University. He worked as a vice president at Intel. Prior to Intel, he worked as a CEO for Chips and Technologies. He received his MSEE degree from Brigham Young University.

**Responsibilities:** He will review the report and make sure that the report meets the university standards for a Masters Project.

2.3.2.2 Industrial Sponsor: Ms. Vanita Corera

**Background:** Ms. Vanita Corera is currently working for the Intellectual Property Business group in L&T Infotech. She has been with L&T Infotech for the past 7.5 years focusing on business development, account management and customer relationship management for wireless and semiconductor OEM/ODM customers across the globe. She holds a Bachelor of Engineering degree in Electronics & Communications and MBA in Marketing Management & IT.

**Responsibilities:** Ms. Vanita Corera helps us in the economic analysis and making of the business model for this product.

3. Literature Review

A literature survey was performed for better understanding of the evolution and developmental trends of high speed 32-bit embedded microprocessors that are currently on the market and defining the characteristics of Quad Logic.

The literature survey for this project (which is the result of reviewing and analyzing many references) provides a brief history regarding the evolution of 32-bit microprocessors (in terms of speed and price) from 1979 until now. It also provides background on the building blocks of a 32-bit embedded microprocessor, various applications of microprocessors, and comparisons between the microcontroller and microprocessor applications (in terms of performance, size, etc.). The current technology approaches utilized in designing high speed embedded control 32-bit microprocessors
that meet the requirements for high performance are also included. The survey also provides information on general specifications of Quad Logic and the technical approaches that this company is going to utilize compared to its competitors to satisfy the requirements of high performance.

3.1 History

The world’s first 32-bit microprocessor design (which was a CISC type), introduced in 1979 by Motorola, was MC68000 (68K) that had 32-bit architecture but was generally described as a 16-bit microprocessor because of its 16-bit internal and external data paths and 24-bit address space. In recent years, Cast Inc. has introduced its C68000-AHB 32-bit microprocessor derived from MC68000 for a variety of applications including 32-bit data processors, sensors, and high speed control systems. In the mid-1980s, MC68000 was the design used by Apple Lisa, Macintosh, Atari ST, and Commodore Amiga due to its high performance, large memory space, and fairly low price. Motorola introduced its fully 32-bit microprocessor (MC68020) in 1985, but the 68K family faded from the market in the early 1990s due to market saturation by much faster RISC designs (Motorola Inc., 2011; Cast Inc., 2011).

The world’s first fully 32-bit microprocessor, introduced in 1980 by AT&T Bell Labs, was BELLMAC-32A (renamed to WE 32000 in 1984 after the divestiture of AT&T). It was used in the minicomputers of AT&T, the first desktop supermicrocomputer, the first 32-bit laptop computer, and the first book-sized supermicrocomputer (IEEE Global History Network, 2011).

Intel introduced its first 32-bit microprocessor (iAPX 432) in 1981 but was not commercially successful due to its poor performance compare to other Intel’s products existing at that time. Between the years 1988 and 2000, Intel introduced several RISC microprocessors. The RISC design introduced in 2000 was based on the ARM architecture. During the last decade, Intel has introduced three different 32-bit embedded microprocessor models: Core, Xeon, and Atom. The Atom models have around ten times lower power consumption (less than 10 watts) compared to the previously introduced models, Core and Xeon (Intel Inc., 2011).

The first 32-bit RISC microprocessor (ARM) was introduced in 1985 by ARM Holdings (a joint venture between Acorn Computers, Apple Computer and VLSI...
Technology). Since then, this processor has dominated the mobile and embedded systems market due to its low power applications, low price, and small size. In 1994, the ARM7 32-bit embedded microprocessor family (ARM7TDMI-S and ARM7EJ-S) was introduced, which helped in establishing ARM architecture in the digital world. Today, the ARM7 microprocessor family is widely used for simple 32-bit devices by a wide range of ARM partners such as Atmel, Broadcom Corporation, and Cast Inc. ARM partners buy the intellectual property cores (IP cores) and create complete CPUs by combining the ARM cores with some optional parts. The most widely used ARM core is ARM7TDMI designed for mobile and low power electronic devices (ARM Holdings, 2011; EmbeddedCraft, 2011).

Tables 1 and 2 give a summary of the various 32-bit microprocessors and 32-bit embedded microprocessor models introduced since 1979 (All the Cortex processors have ARM7 core).

<table>
<thead>
<tr>
<th>Year</th>
<th>Company</th>
<th>32-bit Microprocessor</th>
<th>Clock speed</th>
<th>Cost (per unit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1979</td>
<td>Motorola</td>
<td>MC68000</td>
<td>4-8MHz</td>
<td>$3.62-11.57</td>
</tr>
<tr>
<td>1980</td>
<td>AT&amp;T Bell Labs</td>
<td>BELLMAC-32A</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1981</td>
<td>Intel</td>
<td>iAPX 432</td>
<td>5-7MHz</td>
<td>-</td>
</tr>
<tr>
<td>1985</td>
<td>Motorola</td>
<td>MC68020</td>
<td>12-33MHz</td>
<td>$10.96-143.97</td>
</tr>
<tr>
<td>1987-1994</td>
<td>Motorola</td>
<td>MC68030</td>
<td>33-50MHz</td>
<td>$21.54-74.55</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MC68040</td>
<td></td>
<td>$56.10-282.10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MC68060</td>
<td></td>
<td>$89.18-458.61</td>
</tr>
<tr>
<td>1989-1994</td>
<td>Intel</td>
<td>80486 series</td>
<td>16-100MHz</td>
<td>$25.96-49.27</td>
</tr>
<tr>
<td>1993-1999</td>
<td>Intel</td>
<td>P5</td>
<td>60-300MHz</td>
<td>-</td>
</tr>
<tr>
<td>1995-2006</td>
<td>Intel</td>
<td>P6</td>
<td>60MHz-2GHz</td>
<td>-</td>
</tr>
<tr>
<td>2000-2004</td>
<td>Intel</td>
<td>NetBurst</td>
<td>1.4-3.6GHz</td>
<td>-</td>
</tr>
</tbody>
</table>
3.2 Background

3.2.1 Differences between a Microprocessor and a Microcontroller

A microcontroller and a microprocessor both contain a central processing unit, though some differences between them. As shown in Figure 3, a microprocessor is a CPU on a single chip, whereas a microcontroller includes a CPU, memory (RAM/ROM/EEPROM), and several I/O devices on a single chip. Microprocessors are general purpose computers, whereas microcontrollers are special purpose computers because microcontrollers are used for specific tasks. However, microprocessors can be used for multiple tasks. A system based on microprocessors is more flexible for design than a system based on microcontrollers. The main use of a microprocessor is as a CPU,
which is the heart of a microcontroller. The major use of a microcontroller is in embedded applications.

![Figure 2. Comparison between microprocessor and microcontroller](image)


### 3.2.2 Block Diagram of 32-bit Microprocessor

A block diagram of a 32-bit microprocessor is shown in Figure 4. A microprocessor contains an ALU, multiplier, barrel shifter, instruction decoder and control logic, register bank, address register, and address incrementer. The function of each unit is described below.
ALU: The ALU is the heart of the microprocessor. It mainly performs three types of operations: arithmetic, logical, and comprehensive. Arithmetic operations include basic mathematical operations. Logical operations are AND, NAND, OR, NOR, and XOR. Comprehensive operations include shift and rotate. As shown in Figure 4, a 32-bit ALU
receives inputs from the register bank and provides output to the register bank after performing operations. This type of ALU architecture is known as “register to register architecture.”

**Multiplier:** The ARM uses the “redix-4 architecture” of multiplier. As shown in the block diagram (Figure 4), 32x8 bit multiplier performs multiplication of two 32-bit data that comes from register. To get the final result of the multiplication, the ALU (for addition) and shifter will also be used. Final output of a 32-bit multiplier is in terms of sum (32-bit) and carry. 8 in 32x8 bit shows that the encoding is performed in group of 8 bits. Multiplication result will be saved in the register bank.

**Barrel Shifter:** The Barrel shifter is basically a “Bit rotating shift register.” It performs a rotating function in the register. After shifting, MSB (Most Significant Bit) will go to the LSB (Least Significant Bit) position in the register. Single bit rotate left function is shown in the figure below. As shown in Figure 5, bit from LSB side will shift left and MSB will go to the LSB.

![Figure 4. Barrel rotate shift register](image)


**Address register:** The address register is also a buffer, which stores addresses. These stored addresses will be used by instructions.
**Address Incrementer:** Function of the address incrementer is to increment or decrement the values of register, which is independent of the ALU.

**Instructions decode and Control logic:** The instructions decode and control logic block shown in Figure 4, convert instructions from machine code to binary code, which generate control and timing signals. These control and timing signals provide directions to other blocks of microprocessor. Control logic fetches the instruction from the memory part by transferring address and read commands. It then decodes the fetched instruction to generate required signal, which executes that instruction.

**Register Bank:** The register bank is basically one type of storage. In the microprocessor, register bank is used to buffer address and data. As shown in the block diagram (Figure 4), the register bank has total 37 registers, which includes 30 “general purpose registers,” one program counter, and 6 status registers. Six status registers include one “current program status register” and five “stored program status registers.” Each register contains 32-bits.

### 3.2.3 Applications of 32-bit Microprocessor

Microprocessors are used for office automation, Communication, and Consumer applications. According to Semiconductor Market Forecasts (2010), below are the application areas of 32-bit embedded microprocessors (Semicast, 2010).

- Automotive Under-the-Hood Electronics
- Automotive Aftermarket
- Enterprise Customer Premises Equipment
- Wireless communication Infrastructure
- Office Equipment and Computer Peripherals
- Wired Games Consoles
- Media Players / MP3 Players
- TVs and Set-top Boxes
- Residential Customer Premises Equipment
- Industrial Automation and Drives
- Chip Cards and Payment Processing
3.3 Technology

There are many different technologies in the market that are used for different processors. Transistor sizes are decreasing day by day. As shown in Figure 6, the gate size of the transistor was 10µm in 1971 that was decreased and was around 1.5µm in 1981. In 1995, transistor size was 0.35µm, whereas the transistor size is around 0.045µm that is 45nm now. Because the sizes of the transistor are decreasing day by day, the same space can contain more number of transistors. For example, in Intel’s core 386 the 1µm technology was used and which had 275,000 transistors. Intel’s “Core 2 Extreme QX9650” uses 800 million transistors, which is around 3000 times more than transistors used in core 386. If Intel uses the same technology for QX9650, then the size of chip can be nearly one square feet and it can consume about 3000W power. But using 45nm technology, CPU consumes only 200W power (Future Publishing Limited, 2007).
Here are some latest technologies that are in use and some new technologies will be used in the future. As shown in Figure 7, 65nm and 45nm technologies are in use at present. The 32nm technology is also under development, whereas the 22nm technology is under research and will be used in the future.
3.3.1 Benefits of the 45nm technology

The 45 nm technology is the today’s latest technology for CMOS designing. Here are some of the benefits of 45nm technology. It improves transistor density, and reduces source-drain and gate leakage power. Since transistor size is smaller for 45nm technology, the chip size is smaller, and the chip can contain more number of transistors. In 45nm technology, transistor switching speed is higher than other technologies. Moreover, less power is required for transistor switching in 45nm technology. So, transistors will not get hot soon and can run on high frequency without any damage. Manufacturing cost of wafer is low because standard sized wafers are used in fabrication and thus, more dies can be fixed in one wafer.

3.3.2 Tools going to be used for designing 32-bit embedded microprocessor

Quad Logic is going to use two tools named Cadence virtuoso IC Design tool and its inbuilt Spectre simulator for design and testing purposes. Cadence virtuoso will be used for designing of CMOS circuit, simulating the circuit, error testing of the circuit, layout designing, DRC (Design Rule Check) testing and LVS (Layout Vs. Schematic) testing. Spectre simulator will be used for testing and analysis.

The following listed embedded microprocessor cores are the advanced microprocessors in the market. These processors deliver the better performance and throughput for many applications in the industry.
Table 3 High Performance Embedded Processor Cores

<table>
<thead>
<tr>
<th>Feature</th>
<th>ARC ARC-270D</th>
<th>ARM Cortex-A8</th>
<th>GateArray LEON3</th>
<th>IBM Power 440S</th>
<th>MIPS 74K</th>
<th>Tensilica XTensa LX2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>ARCCompArt</td>
<td>ARMv7</td>
<td>SPARC V8</td>
<td>Power</td>
<td>MIPS32</td>
<td>Xtensa</td>
</tr>
<tr>
<td>Add. Width</td>
<td>32 bits</td>
<td>32 bits</td>
<td>32 bits</td>
<td>32 bits</td>
<td>32 bits</td>
<td>Yes*</td>
</tr>
<tr>
<td>Synthesizable</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
</tr>
<tr>
<td>Pipeline Depth</td>
<td>7 stages</td>
<td>13 stages</td>
<td>7 stages</td>
<td>17 stages</td>
<td>5 or 7 stages</td>
<td>Yes*</td>
</tr>
<tr>
<td>Pipeline Type</td>
<td>Uniscalar</td>
<td>2-way superscalar</td>
<td>Uniscalar</td>
<td>2-way superscalar</td>
<td>Uniscalar</td>
<td>Yes*</td>
</tr>
<tr>
<td>Inst Execution</td>
<td>In order</td>
<td>In order</td>
<td>In order</td>
<td>Out of order</td>
<td>Out of order</td>
<td>In order</td>
</tr>
<tr>
<td>Branch Predict</td>
<td>Dynamic</td>
<td>Dynamic</td>
<td>—</td>
<td>Dynamic</td>
<td>Dynamic</td>
<td>Dynamic</td>
</tr>
<tr>
<td>L1 Cache</td>
<td>0-64K / D</td>
<td>16-32K / D</td>
<td>0-4MB / D</td>
<td>16-32K / D</td>
<td>0-64K / D</td>
<td>0-32K / D (ECC)</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>L3 Cache</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Scratchpad RAM</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
</tr>
<tr>
<td>16-Bit Instr</td>
<td>ARCompArt</td>
<td>Thumb-2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DSP Extensions</td>
<td>Yes*</td>
<td>Neon</td>
<td>Limited (MAC)</td>
<td>Limited (MAC)</td>
<td>MIPS16e</td>
<td>Yes*</td>
</tr>
<tr>
<td>Java Extensions</td>
<td>—</td>
<td>Jazelle RCT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Config ISA</td>
<td>Yes</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>System Interface</td>
<td>32–64 bits</td>
<td>64–128 bits</td>
<td>32 bits</td>
<td>64–128 bits</td>
<td>32 bits</td>
<td>—</td>
</tr>
<tr>
<td>FPUs</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
</tr>
<tr>
<td>MMU + TLB</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>—</td>
</tr>
<tr>
<td>Privilege Levels</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Debug Interface</td>
<td>JTAG</td>
<td>JTAG</td>
<td>LEON3 DSU</td>
<td>JTAG</td>
<td>EJTAG</td>
<td>JTAG</td>
</tr>
<tr>
<td>Max Core Freq (Process)</td>
<td>700MHz</td>
<td>400MHz</td>
<td>700MHz</td>
<td>&gt;1.0GHz</td>
<td>&gt;1.0GHz</td>
<td>1.6GHz</td>
</tr>
<tr>
<td>Power (Core)</td>
<td>—</td>
<td>0.5mW/MHz</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>0.032-0.046mW/MHz</td>
</tr>
<tr>
<td>Core Size (Process)</td>
<td>0.93mm^2</td>
<td>&lt;3.0mm^2</td>
<td>&lt;20,000 gates</td>
<td>n/a</td>
<td>n/a</td>
<td>—</td>
</tr>
</tbody>
</table>

* Available fully synthesizable or partly structured. *Hard-core version also available. *Some DSP extensions standard, more optional.

3.3.3 Methods used for High Performance

The above chart shows the six different embedded processors build to produce high performance. These processors are available as hardcore, as well as they are fully synthesizable. These processors provide the better throughput and are widely used in many applications. These processors consume less power, but that is not the selling point for these processors as the same companies provide the low power 32-bit processors, but they are slower in performance. The better performance requires some compromise in power consumption criteria.

There are many ways to get the better performance and it is not shared in the above chart. Some of these methods are using the bigger pipeline allowing the higher clock rates, executing the multiple instructions at the same time, and rearranging the
instruction for higher efficiency. The ARM, IBM, and MIPS 32-bit processor cores are some of the processors that use this approach to achieve the better performance (Microprocessor Report, 2008).

The Tensilica and MIPS cores use custom extensions of ISA (Instruction Set Architecture) (Microprocessor Report, 2008). These techniques allow achieving the high performance at a relatively less power consumption and without speeding the clocks.

The other technique is to use the multithreading. The applications that are written to use this feature runs faster on multithreaded processor than single threaded processor. Another option to achieve the higher performance is to use the multi core. The above listed 32-bit microprocessor cores are somewhat usable for multi core integration. Some cores from this list are more favorable for the multi core use compare to other in the list.

The MIPS has introduced the four way symmetric multiprocessing (SMP) to multithreaded processing core that was part of the above list (Microprocessor Report, 2008). Simply using the dual threaded core with four way symmetric multiprocssing enables the eight way SMP. This allows the better performance but the power consumption in such scheme also increases relatively compared to other high speed design approaches.

Tensilica’s Xtensa series has 32-bit architecture that provides Flexible Length Instruction eXtensions (FLIX) to its developer that can handle 15 operations in 64-bit instruction (Microprocessor Report, 2008).

The important factor is the size of core and it is difficult to compare sizes for the above listed cores as these cores have various options and features. The actual core size depends on the layout of this core with these options and features. Hence, it is difficult to compare the sizing relevance in these different processor cores.

### 3.4 Product Specifications

The high speed 32-bit embedded control microprocessor that Quad Logic is planning to design will be using the 45nm technology for its processor, which is the technology that is currently being used for transistors. This technology will allow Quad Logic to place more transistors per unit area compared to other technologies with larger transistor sizes. It will also reduce the delay and improve the speed.
The Quad Logic’s high speed 32-bit embedded control microprocessor is going to be a RISC microprocessor that will execute limited number of simple instructions and require fewer numbers of transistors (i.e. it will have smaller size), but will be very fast and cheap for design and production.

Since currently there are few 32-bit embedded microprocessor designs available in the market with speeds higher than 1 GHz, therefore the speed that Quad Logic is planning to achieve for its 32-bit embedded control microprocessor is going to be over 1 GHz.

To achieve the high performance for the 32-bit embedded control microprocessor, Quad Logic is planning to use the pipeline approach. Using this approach for the design will allow higher clock rates, execution of multiple instructions at the same time and rearranging the instructions for higher efficiency.

4. Design and Implementation

Our 32-bit embedded high speed processor design implementation has custom circuit design approach. In first phase, we defined the architecture and prepared the top level block diagram. The top level logic blocks have been defined to achieve the targeted function and performance from each block of the architecture. In second phase of the processor design, we built the transistor level circuit for each of these logic sub blocks. We used the following tools to build the schematic and size the transistors to achieve targeted speed at sub logic level.

Design and testing tools:

- Cadence “Virtuoso” IC design tool for schematic entry
- Jdsize for device size calculation
- Spectre Spice simulation for testing

These circuits have been functionally verified using the Cadence Simulation tool for the correct timing and logical results. We tested these circuits at smaller logic levels and integrated levels using the Spectre simulation to check and validate the timing and functional results. We debugged and troubleshoot the timing and functional issues from the simulation test results.
4.1 Design Implementation

In this section, we are going to cover the circuit design for major logic blocks in our high speed embedded control processor. This section covers the top level schematic and its functional explanation. It also covers output waveforms to show the test results at block level.

4.1.1. Instruction Decoder

The instruction decoder is the circuit block in the processor unit that takes the op code bits from the instruction and translates them into the required control signal to complete the required instruction. The ALU control signals set the ALU to do arithmetic or logical function. The memory and register related control signals sets memory to read or write operation based on the op code in the instruction. The instruction decoder has two elements: First is pre-decoder section and second is ROM section. The pre-decoder section decodes the op code and generates the single decoder output. This pre-decoder signal output goes into the ROM and reads the prewired control bits. The following figure shows the top level schematic of Instruction Decoder.

![Figure 7. Top level schematic of Instruction Decoder](image)

We have designed pre-decoder for Dynamic logic. The pre-decoder circuit takes one phase of clock. In schematic, op code bits and bits_bar are connected to Dynamic
AND gate. Figure 9 shows the blow up section of the pre-decoder circuit. The ROM is also exercised in Dynamic logic and it requires one phase of clock to get the output. In ROM, the control bits and pre-decoder output are tied down to FET that is hardwired. Figure 10 shows the magnified section of Dynamic ROM. The complete Instruction Decoder table is given in Appendix A.
4.1.2. Barrel Shifter

The Barrel shifter is the circuit block in the processor that shifts the data by specified number of bits. The instruction carries the 5-bit code that specifies the number of bits to be shifted. The shifter is designed to shift data bits logically and arithmetically either left or right. In logical left shift, the barrel shifter will shift the data bits by specified number of bits to more significant positions and the result has lower significant bits that are filled with zeros. In logical right shift, the barrel shifter will shift the data bits by specified number of bits to lower significant bits and the result has higher significant bits that are filled with zeros.

The main circuit block for the barrel shifter is build based on the MUX circuit. Our 32-bit shifter has five stages of MUX hierarchy. These five stages do the shift part of the operation. There are totally five control bits that specify the shift amount of 0 to 32-bit. Each stage is connected to one control line. The first stage has control bit S0 that controls the shift by one, the second stage has control bit S1 that controls the shift by two, the third stage has control bit S2 that controls the shift by four, so on so forth. The output of each stage is wired to input of next stage in such a way that it will logically follow the shift control specified through the five control lines. We have added two more stages that basically decide the shift direction. First stage is added in the beginning and second stage
is added in the last. These two stages are connected to the same control line that controls the direction either left or right. The output and input of these two stages are wired in such a way that upon getting the right shift control they reverse the data input in beginning and end stage to help the shift in right direction.

Figure 10. Barrel shifter schematic diagram
The waveform below is the output of the test bench that we run on designed barrel shifter with fixed 32-bit input codes of all 1’s and control bits connected to generate all 32 combination of five bit code in sequence. The waveform picture shows shift left output that at each clock cycle and each lower significant bit of the result it is filled with zeros.

Figure 11. Barrel shifter shift left output waveforms
4.1. 3 D-Cache

In our processor architecture, we have used 32-bit wide and 16K deep SRAM memory for Data cache purpose. Our D-Cache memory has 32 pages and each page has 512 lines. The following circuit shows the top level circuit diagram of D-cache memory. There is a dynamic address decoder circuit block that takes 9-bit of address information and generates the 512 decoder output that connects to SRAM memory page which is 32-bit wide with 512 lines. The decoder output selects the particular memory line based on the memory address bits for reading or writing operations in SRAM memory. There is separate read and write circuit inside the SRAM page. There is separate 32-bit register set used for data input and output register.

![Figure 12. D-Cache top level schematic](image-url)
4.1.4 I-Cache

In our processor architecture, we have used four instructions wide (32X4 bit=128 bit wide) and 16K deep SRAM memory for Instruction cache (I-cache) purpose. The instruction cache consists of 32 pages and each of this memory pages has 512 lines. The following circuit shows the top level circuit diagram of I-cache memory. I-Cache page requires the same decoder logic to decode, which takes 10-bit of address input, and decodes into 512 outputs. Hence, we have used the same dynamic decoder circuit logic that has been used in D-Cache. The decoder output selects the particular memory line based on the memory address bits for reading or writing operations in SRAM memory.

There is a separate read and write circuit inside the Static SRAM page. There is a separate 32-bit register set used for data input and output register.

![I-Cache top level schematic](image)

Figure 13. I-Cache top level schematic

I-cache is four instructions wide and it can read or write four 32-bit instructions at the same time and hence, delivers better throughput that is in line with the throughput of the rest of the logic on the processor.
4.1.5 ALU

ALU (Arithmetic and logical unit) is one of the major blocks of the microprocessor. ALU performs arithmetic and logical operations, such as addition, subtraction, shifting, rotation etc. It takes the control signals from decoder and performs different arithmetic and logical functions accordingly. Output of the ALU goes to memory and program counter. Figure 15 is showing the top level diagram of the ALU. As shown in Figure 15, ALU is made up of different elements, but propagate, generate, and XOR are vital blocks of the ALU.

Figure 14: Top level schematic of ALU

Inputs of the ALU are connected with the plus-minus block. Plus-minus block is basically used for sign bit operations. As shown in the figure 15, outputs of the plus-minus block are connected with propagate and generate blocks. As we have designed 32-bit ALU, design contains 32 propagate and 32 generate blocks. 32 propagate and generate blocks are divided into 8 group propagate and group generate blocks respectively.
Similarly, 8 group propagate and group generate blocks are further divided into two section propagate and section generate blocks respectively. Carry blocks are mainly used to generate and carry out the carry bit. Bit carry, group carry and section carry blocks get inputs from propagate-generate, group propagate-generate and section propagate-generate blocks respectively.

Circuit diagram of propagate and generate are shown in Figures 16 and 17, respectively. In propagate and generate blocks S0 to S7 are the control bits, where as a_out, ab_out, b_out and bb_out are the input data bits. Input data bits perform operations according to the control bits that come from the decoder. Some of the sample control bit combinations are showed in the following look up table. Outputs of propagate and generate are p and g, respectively.

Table 4: Look Up table for ALU

<table>
<thead>
<tr>
<th>Control Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CI</td>
<td>S0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Figure 15: Circuit diagram of Propagate

Figure 16: Circuit diagram of Generate
To test the ALU block, we have performed the subtraction function. As shown in the look up table 5, for subtraction (A-B) we have used control bits S0 to S7.

Table 5: Look up table for subtraction

<table>
<thead>
<tr>
<th>Control Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0  S1  S2  S3  S4  S5  S6  S7  CI</td>
<td>Subtraction(A-B)</td>
</tr>
<tr>
<td>1   0   0   1   0   0   1   0   1</td>
<td></td>
</tr>
</tbody>
</table>

We have subtracted 13 from 44, so we got the result = 31 that is shown in the following graph. As we have used many different blocks in ALU, it takes 11 evaluate cycle to execute the operation. We are getting the output of the ALU after 11 evaluate cycles that is shown in Figure 18.

Figure 17: Output wave forms of ALU
4.1.6 Program Counter

The Program Counter (PC), which is a 32-bit register inside the microprocessor, holds the memory address of the next instruction that has to be executed. After the microprocessor reads the stored address of the executing instruction from the PC, the fetched address is decoded. Then, the processor executes the instruction and the PC is updated to store the address of the next instruction in memory (Haung, 2009; Microprocessor and Memory Basics, 2006).

According to the architecture of the memory, which has been described earlier, the circuit for updating the PC has been constructed. Figure 19 shows the block diagram of the program counter circuit. The program counter receives its inputs (D) from the Adder. The outputs (Q) of the PC, which determine the address of the next instruction, are the outputs of the flip-flops, which are the major building blocks of the PC. The reset input forces the PC to 0 and then, reading the instruction address starts (Haung, 2009; Microprocessor and Memory Basics, 2006). Figure 20 shows the top level schematic of the program counter circuit.

![Figure 18. Block diagram of the program counter circuit](image)

Figure 18. Block diagram of the program counter circuit
Our microprocessor is a 32-bit RISC processor therefore, all the instructions have the same length of 32-bits and the PC is incremented by 4 bytes at each clock cycle. Furthermore, two conditional situations can be dictated to the PC through using branch and Jump signals, and the PC can move to a different instruction address instead of being incremented after fetching each 4 bytes of instruction. If the Branch signal is 1 then, having a new address by adding or subtracting a value to the current address is being dictated to the PC but, if the Jump signal is 1 then, discarding the previous address and accepting the new address is being dictated to the PC. The Branch and Jump conditional situations are made through using MUX (Haung, 2009; Microprocessor and Memory Basics, 2006).

The 32-bit program counter (Figure 21a) designed for the microprocessor consists of four 8-bit program (Figure 21b) counters and each of these 8-bit PCs are made from eight D type flip flops (Figure 21c). Figure 3 shows the transistor level schematic of the D flip flop whose output is the same as its input.
Figure 20. Top level schematic of (a) 32-bit PC, (b) 8-bit PC and (c) D flip flop

Figure 22 shows a sample result of the program counter function during the time period of 5ns. As can be seen, the six sample output signals (22a) of the PC follow their related input signals (22b).
Figure 21. Six sample PC outputs (a) and their related inputs (b)
4.2 Implementation Result

In this section, we are showing the three key test results that directly connected with our high speed embedded control 32-bit microprocessor. We have run various test and simulations to check and validate the performance and speed. We have done the transistor count in our 32-bit embedded high speed processor design to show the effective use of number of transistors that directly relates to the effective die size.

4.2.1 Transistor Count

We have used 45nm node technology in our design. We have precisely sized each transistor to achieve the desired speed and none of the transistors in the circuit is oversized. The custom transistor sizing allows the effective and precise use of silicon wafer space during the layout phase. In our design, the total transistor count is around 1 million that includes the transistor count for I-cache and D-cache, which take the maximum number of transistors. The good thing is that these SRAM memory cell transistors are the minimum size transistors. The table below shows the transistor count for various key logic sections in our processor.

<table>
<thead>
<tr>
<th>Processing Logic Section</th>
<th>Transistor Count</th>
<th>Memory Section</th>
<th>Transistor Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Block</td>
<td></td>
<td>SRAM block</td>
<td></td>
</tr>
<tr>
<td>ALU</td>
<td>4467</td>
<td>I-cache (128bit wide x 16K)</td>
<td>786432</td>
</tr>
<tr>
<td>Adder</td>
<td>2899</td>
<td>D-cache (32-bit wide x 16K)</td>
<td>196608</td>
</tr>
<tr>
<td>Barrel Shifter</td>
<td>1810</td>
<td>Registers</td>
<td>6144</td>
</tr>
<tr>
<td>Address Decoder</td>
<td>11242</td>
<td>Total</td>
<td>989184</td>
</tr>
<tr>
<td>Program Counter</td>
<td>448</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dummies</td>
<td>2240</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>23106</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4.2.2 Speed and performance result

We have performed various simulations on the integrated processor circuit to check the functionality and timing. We have run the simulations for data processing instructions. The data processing instruction includes the ALU operation for arithmetic functions, like addition, subtraction and logical functions, like increment, decrement, XOR, AND, etc. The simulation results are checked for the correct functional output and timing outputs. The following test and simulation waveforms clearly indicate that our high speed 32-bit embedded microprocessor is running at 1.5 GHz speed.

Figure 22. Data processing instruction simulation results

The above simulation results shows the result for subtract data processing operation. We are getting the first output after latency of 2ns and every 660ps we are getting the valid data out from the ALU. The 660ps in time domain is equal to 1.5 GHz speed. This confirms that our processor produces the valid function data processing results at 1.5 GHz speed.
5. Economic Analysis

5.1 Executive Summary

The demand of handheld computing device is growing with addition of many functions and applications. The present choice of processor are not completely meeting the need and relatively expensive. The market needs the efficient high speed and performance application processor.

- Quad logic has deployed the custom transistor sizing, four stage pipeline, and incorporated I-cache and D-cache to meet the handheld computing device need.
- Quad logic is providing this efficient processor IP at relatively low cost. The effective cost to use this custom solution IP ranges from $2.25 per device to $0.88 per device based on making number of device using our IP.
- Handheld computing device and smart phone manufacturers like Nokia, Vizio, LG, Samsung, Motorola, Sony, and ST- Ericson are potential customers for our processor IP.
- The smart phone total users will be 1.7 billion by 2014 (Market Research, 2010).
- Quad Logic needs total 3.2 million dollar investment that will produce 56 million dollar balance cash by end of year 2016.
- Quad Logic will breakeven in Q2 of 2013.
- The Return on Investment by the year 2016 is 177%.

5.2 Problem Statement

The demand of handheld computing device with more features and application is going to grow which requires the better supporting application based microprocessor. The current 32-bit embedded microprocessor series does not completely meet the market demand for the mobile computing market. The solution needs to solve the key requirements of the performance and price. The solution should provide the flexibility to application programmer to handle the larger applications.
5.3 Solution and Value Proposition

The 32-bit embedded microprocessor of Quad Logic is designed to meet the high speed, the high performance, and the large application needs of mobile computing devices. The approach used to meet each of these requirements is described below.

Quad Logic used 45nm technology to achieve its high speed design. Each and every transistor in the design is precisely sized using 45nm technology to meet the high speed. In addition, the design is developed in such a way that the logic is reduced to build with fewer transistors so that the design reduces the logic delay and improves the speed of the design.

Quad Logic developed the 32-bit microprocessor design with the four stage pipeline process to achieve high performance. The pipeline process of instruction execution enables the design to execute multiple instructions back to back so that the throughput is much higher than the standard instruction execution.

Quad Logic used internal memory of I-Cache and D-Cache to meet the large application needs of mobile computing devices. The internal cache memory provides more flexibility and resources to the applications. I-Cache and D-cache are also designed with SRAM, which is much faster and consumes low power.

With all the above approaches, Quad Logic’s 32-bit embedded microprocessor runs at speeds higher than 1GHz. There are very few 32-bit embedded microprocessors that run at speeds higher than 1GHz in the market. However, those microprocessors are more expensive. Quad Logic offers a much better solution to address the market needs of mobile computing devices at a comparable price. Quad logic provides this processor IP which will cost $ 2.25 per device to our customer when they make 300k devices. This cost goes down to $0.88 with 10,000k devices.

Quad Logic provides the high speed and performance application processor at very reasonable price and solves the application programmer need.

5.4 Market Size

Report of Global Microprocessor, 2010, says that the annual delivery of 32-bit microprocessors is over 180 million units, which is increasing by 22% annually (Electronic Engineering Business Plan, 2011). According to a market research firm, 33% is the consumer market as shown in the figure below. The manufacturers sell current 32-
bit embedded processors mostly for the consumer application market first, then they go to communication and office automation markets (Market Research, 2010). The key demand of this market is to have a high level of integration and performance with cost effective solutions.

![32-bit Microprocessor Market Distribution Chart](image)

Figure 23. Market distribution chart

The major consumer market for 32-bit embedded microprocessors is mobile computing, which is in heavy demand and is widely used now. It is forcing the semiconductor industry to set the strategy for the future demand. Smart phones now have powerful processing power with 1GHz speed and gigabyte of storage space. It is challenging to cover all the aspects like processing power, speed, power consumption, and battery management in microprocessor design. The same processor is now used in netbooks and tablet devices.

According to Martin Hingley, the number of mobile phone units shipped is 1.33 billion, which is worth of $191 billion by Q1 of 2011 in the year. Out of these, the number of smartphone units shipped is 235 million, which is worth of $84 billion as shown in the figure below.
Nokia is shipping more number of units (28%), where as Apple (44.2%) leads the smartphone revenues. According to Martin Hingley’s forecast, the number of smartphones shipped will be 377 million, which will be worth of $153 billion in 2016.

The emerging market and extensive purchase in Asian countries like China, India, and Central and Latin America, indicates that the number of smartphone users are going to reach 1.7 billion by 2014 (Market Research, 2010). Based on the research and the emerging countries’ market demand, there will be a huge demand for mobile computing devices, such as smart phones, tablet devices, and networking products. This is the key growth indication in the 32-bit embedded microprocessor market.

5.5 Competitors

Competitors in the 32-bit embedded microprocessor market are some of the major semiconductor companies, like Texas Instruments, AMD, ARM, Marvel, Freescale, Nvidia, etc. There are a few small companies that are providing 32-bit embedded
microprocessor IP. The following table shows the speed, power, and price of different 32-bit embedded processors in the market.

Table 7 Competitors of 32-bit embedded microprocessor

<table>
<thead>
<tr>
<th>32-bit embedded processor</th>
<th>Speed</th>
<th>Power</th>
<th>Price per Unit (minimum 100 pieces in quantity)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARC 750D</td>
<td>700 MHz</td>
<td>40 µW/MHz</td>
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The competition, as well as the growth for the 32-bit embedded microprocessor market is huge. According to Barber Analytics (2011), “the biggest market for processor IP providers, however, is mobile handsets. Total handset sales volume worldwide was approximately 1.1 billion units in 2007 with most of the growth coming from Smart phones and the sale of low end handsets in India and China. ARM dominates the handset segment with approximately 80% market share.” (p. 1).

5.6 Customers

Based on the research and the emerging countries’ market demand, we are targeting the customers in mobile computing devices, such as smart phones, tablet devices, and networking products.

According to IMS research as shown in the figure below, the smart phone sales would be 28% of the total mobile handset sales during 2011. Nokia sold 40% of the smartphones in Q1 of 2010, whereas the number dropped to 24% in Q1 of 2011. However, Apple is gaining the number of units by 3% from Q1 of 2010 to Q1 of 2011. Samsung’s share is rising rapidly from 3% to 13%.

![Smartphone Market Share Estimates - 1Q10/1Q11](image)

Figure 25. Smart phone market share estimates (Q1 2010 to Q1 2011)

The above figures indicate that Google and Apple are the major companies in the US smart phone market, where as Google and Nokia are the major companies in the worldwide smart phone market. According to the age groups market analysis, ages 25-34 use smart phones more than other age groups.

According to the article by Trent Nouveau (2011), Apple’s iPad will dominate the market in tablet devices till 2015. From the table below, the market share of Apple’s tablet is 83.9% and Google’s share is 14.2% in 2010.
Table 8  Worldwide sales of Media Tablets

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<th>OS</th>
<th>2010</th>
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<th>2012</th>
<th>2015</th>
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<td>14,766</td>
<td>47,964</td>
<td>68,670</td>
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<td>Market Share (%)</td>
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<td>Market Share (%)</td>
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<td><strong>Total Market</strong></td>
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<td><strong>69,780</strong></td>
<td><strong>108,211</strong></td>
<td><strong>294,093</strong></td>
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</table>

Source: Gartner (April 2011)


With the above market survey, the major market and growth for 32-bit embedded microprocessors is in smart phones, tablet devices, and netbooks. Quad Logic would mainly focus on smart phone and tablet device customers, such as Nokia, Vizio, LG, Acer, Google, Samsung, Motorola, ST-Ericsson, Toshiba, Sony, Philips, etc.

5.7 Cost Analysis

Various costs are involved in developing our microprocessor IP. Some of these costs are fixed and some are variable costs. Variable costs include employee salaries, infrastructure costs, CAD tools costs, and Marketing/Sales promotion cost. All other
costs, such as, rent/lease costs, patent and legal costs, utilities costs, transportation costs, etc., are fixed costs. The sections below describe more details on each of these costs.

5.7.1 Variable costs

5.7.1.1 Employee Salary costs

Employees are the key to any organization. We offer good pay structure to our employees. The pay structure includes base salary and benefits. The benefits are given in different ways. Each employee is eligible to receive health insurance to the employee’s family as well. We also offer stock options and performance based incentives. The benefits cost approximately 30% of the employee salary. Quad Logic also hikes the salaries regularly. We are planning to give the first salary hike in Q1 of 2014, by which we are expecting a return on our investments. The salaries and the benefits of each employee are shown in the following table.

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<td>16.5</td>
<td>18</td>
<td>18</td>
<td></td>
</tr>
</tbody>
</table>
5.7.1.2 Infrastructure costs

Infrastructure costs include the expenses for computers, chairs, desks, printers, and high end compute servers. The number of computers and chairs are added based on the number of employees. We need high end compute servers with high speeds and large memory to execute simulations of our IP. We would be starting with three servers initially and are planning to increase based on customer growth later on. The annual infrastructure cost is shown in the following table.

Table 10. Annual Infrastructure costs

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Computers</td>
<td>Number of Units</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>cost of one unit (k$)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>Total in K$</td>
<td>4.0</td>
<td>2.0</td>
<td>1.0</td>
<td>1.2</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>High end compute servers</td>
<td>Number of Units</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>cost of one unit (k$)</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>Total in K$</td>
<td>7.5</td>
<td>0</td>
<td>0</td>
<td>11</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Chairs and desks</td>
<td>Number of Units</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>cost of one unit (k$)</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>Total in K$</td>
<td>1.2</td>
<td>0.6</td>
<td>0.3</td>
<td>0.6</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>Printer</td>
<td>Number of Units</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>cost of one unit (k$)</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>Total in K$</td>
<td>2.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td></td>
<td>Total in K$</td>
<td>14.7</td>
<td>2.6</td>
<td>1.3</td>
<td>12.8</td>
<td>1.2</td>
<td>1.2</td>
</tr>
</tbody>
</table>
5.7.1.3 CAD tools cost

We are performing the circuit design and testing using Cadence Virtuoso tool. The Virtuoso package contains various modules, such as Spectre simulator, analog design environment, Virtuoso XL, layout suite, etc., needed for our IP development. We are initially planning to get three licenses of the Virtuoso package during the main design and testing phase. We would like to retain the same number of licenses till the end of 2012 and are planning to increase the number of licenses from 2013 onwards. The following table shows an expected annual CAD tool cost.

Table 11 CAD tool cost

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Cadence CAD tool</td>
<td>Number of new licenses</td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Virtuoso CAD tools cost per license (K$)</td>
<td>120</td>
<td>0</td>
<td>120</td>
<td>125</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Maintenance (K$)</td>
<td>0</td>
<td>576</td>
<td>648</td>
<td>696</td>
<td>768</td>
<td>768</td>
</tr>
<tr>
<td></td>
<td><strong>Total in K$</strong></td>
<td><strong>360</strong></td>
<td><strong>576</strong></td>
<td><strong>768</strong></td>
<td><strong>821</strong></td>
<td><strong>768</strong></td>
<td><strong>768</strong></td>
</tr>
</tbody>
</table>

5.7.1.4 Marketing and Sales Promotion cost

After the employee salary cost, the next major expense is the marketing and sales promotion cost. Since Quad Logic is a startup company, we need more advertisement and promotions to advertise our IP in the market. Also, the sales team would be travelling more to bring more customers. The traveling cost also contributes a major expense. We are considering 20% of our revenue for the marketing and sales promotion expenses. The following table shows the annual marketing and sales promotion cost.

Table 12 Marketing and sales promotion cost

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Advertisement and Promotion cost (K$)</td>
<td>35.1</td>
<td>299.565</td>
<td>549.875</td>
<td>718.2</td>
<td>995.995</td>
<td>1022.23</td>
</tr>
<tr>
<td>Travel(K$)</td>
<td>25</td>
<td>150</td>
<td>300</td>
<td>412.5</td>
<td>450</td>
<td>450</td>
</tr>
<tr>
<td>-----------</td>
<td>----</td>
<td>-----</td>
<td>-----</td>
<td>-------</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>Total in K$</td>
<td>60.1</td>
<td>449.565</td>
<td>849.875</td>
<td>1130.7</td>
<td>1445.995</td>
<td>1472.23</td>
</tr>
</tbody>
</table>

5.7.2 Fixed costs

5.7.2.1 Patent and Copyright costs

Quad Logic is planning to file a patent to protect our design. We are expecting the design to be completed by Q2 of 2012. We are planning to file a provisional patent with the United States Patent and Trademark Office (USPTO) in Q4 of 2012 to have the priority filing date. We understand that the provisional application is valid for 12-months, in which a non-provisional full patent should be submitted to protect the invention. The fee for the provisional application is very minimal (around $250). Thus, we want to file a provisional application first and then we have 12-months of period to assess the potential of our invention in the market before filing the full patent. Right now, we are planning to file the full patent in Q2 of 2013. The filing fee for a full patent depends on the number of parameters, such as number of independent claims, number of dependent claims, number of total claims, surcharge, etc. We are expecting the full patent fee to cost around $20,000. We are also planning to apply for copyright on our design document in Q1 of 2012.

Table 13 Annual Patent and Copyright costs

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Provisional patent filing cost (k$)</td>
<td>0</td>
<td>0.5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Full patent filing cost (k$)</td>
<td>0</td>
<td>0</td>
<td>20</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Copyright in (k$)</td>
<td>0</td>
<td>0.05</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Legal Consultant cost (k$)</td>
<td>0</td>
<td>10</td>
<td>22</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total in K$</td>
<td>0</td>
<td>10.55</td>
<td>42</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
5.7.2.2 Lease/Rent cost

We will be leasing an office space for our company in Santa Clara, California, USA. The office space in Santa Clara will cost us about $20 per sq ft/year. We are planning to lease a space of 6000 square feet area. We will be expanding or moving to new location based on our growth. The following table gives more details about the lease and the rent.

Table 14 Lease/Rent cost

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Lease Advance</td>
<td>Per 12 months</td>
<td>80</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(k$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rent</td>
<td>Per month</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>27.5</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>(K$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Annual (k$)</td>
<td>60</td>
<td>240</td>
<td>262.5</td>
<td>352.5</td>
<td>420</td>
<td>420</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total in K$</td>
<td></td>
<td>140</td>
<td>240</td>
<td>262.5</td>
<td>352.5</td>
<td>420</td>
<td>420</td>
</tr>
</tbody>
</table>

5.7.2.3 Overhead costs

Various other overhead costs will incur every month based on the usage. The following table shows all other overhead costs, such as internet and phone, utilities, stationary, miscellaneous, etc.

Table 15 Overhead costs

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Internet and Phone</td>
<td>2</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>(K$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Utilities (K$)</td>
<td>2</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>15.25</td>
</tr>
<tr>
<td>Stationary (K$)</td>
<td>0.25</td>
<td>1</td>
<td>2</td>
<td>2.5</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Miscellaneous (K$)</td>
<td>2.5</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>
Total in K$ | 6.75 | 27 | 32 | 36.5 | 42 | 42.25

5.7.3 Total cost

We have calculated the total cost that our company will need to spend every year to develop the 32-bit embedded microprocessor IP. The following table shows the yearly expenses.

Table 16 Total cost

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Employee Salaries (K$)</td>
<td>292.5</td>
<td>2139.75</td>
<td>2746.75</td>
<td>3591</td>
<td>4527.25</td>
<td>4646.5</td>
</tr>
<tr>
<td>Infrastructure Cost (K$)</td>
<td>14.7</td>
<td>6.65</td>
<td>1.95</td>
<td>14.6</td>
<td>3.6</td>
<td>2.4</td>
</tr>
<tr>
<td>Patent and Copy right cost (K$)</td>
<td>0</td>
<td>10.55</td>
<td>42</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Rent/Lease Cost (K$)</td>
<td>140</td>
<td>240</td>
<td>262.5</td>
<td>352.5</td>
<td>420</td>
<td>420</td>
</tr>
<tr>
<td>CAD tools cost (K$)</td>
<td>360</td>
<td>576</td>
<td>768</td>
<td>821</td>
<td>768</td>
<td>768</td>
</tr>
<tr>
<td>Marketing and Sales promotion cost (K$)</td>
<td>60.1</td>
<td>449.565</td>
<td>849.875</td>
<td>1130.7</td>
<td>1445.995</td>
<td>1472.23</td>
</tr>
<tr>
<td>Overhead cost (K$)</td>
<td>6.75</td>
<td>27</td>
<td>32</td>
<td>36.5</td>
<td>42</td>
<td>42.25</td>
</tr>
<tr>
<td>Total cost in K$</td>
<td>874.05</td>
<td>3449.515</td>
<td>4703.075</td>
<td>5946.3</td>
<td>7206.845</td>
<td>7351.38</td>
</tr>
</tbody>
</table>

The following figure shows the total cost that our company will need to spend every quarter till the end of 2015.
The figure below shows the pie chart of all the total expenses till the end of 2015. It reveals that the major expenses are the employee salaries, which is costing 60% of the total expenses. The marketing and sales promotion is costing 18%, whereas the CAD tools are costing 15% of the total expenses.
Figure 28. Pie chart of Total expenses

5.8 Price Point

The table below shows the price of the similar 32-bit embedded microprocessors in the market. The unit price shown is for the microprocessor chip and not for the IP licensing. Quad Logic is a fab-less Semiconductor Company and will be licensing the IP alone. Based on our revenue calculation, we are expecting revenue of $1.28 million for 600,000 units sold. As a result, the IP licensing costs only around $2.0 per unit to our customers, which is much below the price charged by our competitors.
Table 17 Price point

<table>
<thead>
<tr>
<th>Company name</th>
<th>Model</th>
<th>Unit price (in $)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM</td>
<td>Cortex A8 (XAM3894CYG)</td>
<td>71.12</td>
</tr>
<tr>
<td>Broadcom</td>
<td>BCM125</td>
<td>300-400</td>
</tr>
<tr>
<td>IBM</td>
<td>PPC 750G</td>
<td>105</td>
</tr>
<tr>
<td>Freescale</td>
<td>MPC744</td>
<td>47-332</td>
</tr>
<tr>
<td>Freescale</td>
<td>MPC856</td>
<td>104-140</td>
</tr>
<tr>
<td>PMC-Sierra</td>
<td>RM9000x2G</td>
<td>321</td>
</tr>
</tbody>
</table>


5.9 SWOT Assessment

Quad Logic analyzed its strengths, weaknesses, opportunities, and threats (SWOT) for developing the strategies. This SWOT analysis will include several areas, such as marketing, technology, research, finance, customers, and competitors.

The strengths of Quad Logic’s 32-bit embedded control microprocessor will be its higher speed and higher performance, and comparable cost. The weaknesses are first, Quad Logic is a startup company in the current recession period and second, it has limited number of financial resources. The opportunity for Quad Logic is the fast growing market demand for high speed 32-bit embedded control microprocessors, but the new designs of the competitors can be a threat to this startup company.

5.10 Investment Capital Requirements

The break even point is the point where a company is neither making profit nor losing any money. Break Even Analysis is very important for any company as it gives the lower limit of profit when you are deciding the margins. It is important to precisely forecast the expected costs and sales to arrive at the accurate break even point. We have calculated break even point by considering the expenses and revenues at each quarter as shown in the table below.
Table 18 Quarterly expenses and revenues

<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Fixed Cost (in K$)</th>
<th>Variable Cost (in K$)</th>
<th>Total Cost (in K$)</th>
<th>Total Revenue (in K$)</th>
<th>Profit (in K$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>Q4-2011</td>
<td>194</td>
<td>680</td>
<td>874</td>
<td>0</td>
<td>-874</td>
</tr>
<tr>
<td></td>
<td>Q1-2012</td>
<td>219</td>
<td>526</td>
<td>745</td>
<td>0</td>
<td>-745</td>
</tr>
<tr>
<td></td>
<td>Q2-2012</td>
<td>240</td>
<td>588</td>
<td>828</td>
<td>350</td>
<td>-478</td>
</tr>
<tr>
<td></td>
<td>Q3-2012</td>
<td>274</td>
<td>652</td>
<td>926</td>
<td>420</td>
<td>-506</td>
</tr>
<tr>
<td></td>
<td>Q4-2012</td>
<td>270</td>
<td>681</td>
<td>950</td>
<td>420</td>
<td>-530</td>
</tr>
<tr>
<td>2012</td>
<td>Q1-2013</td>
<td>306</td>
<td>767</td>
<td>1073</td>
<td>675</td>
<td>-398</td>
</tr>
<tr>
<td></td>
<td>Q2-2013</td>
<td>328</td>
<td>821</td>
<td>1149</td>
<td>1280</td>
<td>131</td>
</tr>
<tr>
<td></td>
<td>Q3-2013</td>
<td>296</td>
<td>947</td>
<td>1243</td>
<td>1605</td>
<td>362</td>
</tr>
<tr>
<td></td>
<td>Q4-2013</td>
<td>296</td>
<td>941</td>
<td>1238</td>
<td>2880</td>
<td>1642</td>
</tr>
<tr>
<td>2013</td>
<td>Q1-2014</td>
<td>364</td>
<td>1053</td>
<td>1417</td>
<td>3200</td>
<td>1783</td>
</tr>
<tr>
<td></td>
<td>Q2-2014</td>
<td>364</td>
<td>1041</td>
<td>1405</td>
<td>3760</td>
<td>2355</td>
</tr>
<tr>
<td></td>
<td>Q3-2014</td>
<td>364</td>
<td>1197</td>
<td>1561</td>
<td>4640</td>
<td>3079</td>
</tr>
<tr>
<td></td>
<td>Q4-2014</td>
<td>364</td>
<td>1199</td>
<td>1563</td>
<td>5200</td>
<td>3637</td>
</tr>
<tr>
<td>2014</td>
<td>Q1-2015</td>
<td>370</td>
<td>1350</td>
<td>1720</td>
<td>5335</td>
<td>3615</td>
</tr>
<tr>
<td></td>
<td>Q2-2015</td>
<td>370</td>
<td>1422</td>
<td>1793</td>
<td>6360</td>
<td>4567</td>
</tr>
<tr>
<td></td>
<td>Q3-2015</td>
<td>370</td>
<td>1458</td>
<td>1829</td>
<td>6670</td>
<td>4841</td>
</tr>
<tr>
<td></td>
<td>Q4-2015</td>
<td>370</td>
<td>1495</td>
<td>1865</td>
<td>6870</td>
<td>5005</td>
</tr>
<tr>
<td>2015</td>
<td>Q1-2016</td>
<td>371</td>
<td>1494</td>
<td>1865</td>
<td>7710</td>
<td>5845</td>
</tr>
<tr>
<td></td>
<td>Q2-2016</td>
<td>371</td>
<td>1494</td>
<td>1865</td>
<td>7995</td>
<td>6130</td>
</tr>
<tr>
<td></td>
<td>Q3-2016</td>
<td>371</td>
<td>1532</td>
<td>1902</td>
<td>8415</td>
<td>6513</td>
</tr>
<tr>
<td></td>
<td>Q4-2016</td>
<td>371</td>
<td>1531</td>
<td>1901</td>
<td>8460</td>
<td>6559</td>
</tr>
</tbody>
</table>

The graphical chart is the best way to show the breakeven point. The simplest way to find the breakeven point is the intersection of expense and revenue lines. The following graph shows the Quad Logic break even analysis. The Chart indicates that Quad Logic will breakeven at Q2 of 2013.
The table below shows the expenses till the breakeven point (Q2 of 2013). We need an investment capital of $9.0 million till the breakeven point. The initial funding for the company is mostly the self-investment. The initial investment would be spent for the IP development expenses, such as labor, office rent, infrastructure, CAD tools, etc.

Table 19  Total cost till breakeven

<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Expenses (in K$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>Q4-2011</td>
<td>874.05</td>
</tr>
<tr>
<td>2012</td>
<td>Q1-2012</td>
<td>744.96</td>
</tr>
<tr>
<td></td>
<td>Q2-2012</td>
<td>828.18</td>
</tr>
<tr>
<td></td>
<td>Q3-2012</td>
<td>926.375</td>
</tr>
<tr>
<td></td>
<td>Q4-2012</td>
<td>950</td>
</tr>
<tr>
<td>2013</td>
<td>Q1-2013</td>
<td>1072.86</td>
</tr>
<tr>
<td></td>
<td>Q2-2013</td>
<td>1149.185</td>
</tr>
<tr>
<td></td>
<td>Q3-2013</td>
<td>1243.468</td>
</tr>
<tr>
<td></td>
<td>Q4-2013</td>
<td>1237.563</td>
</tr>
<tr>
<td></td>
<td>Total cost till breakeven (in K$)</td>
<td>9026.64</td>
</tr>
</tbody>
</table>

Figure 29. Break even analysis
5.11 Personnel

Our organizational structure, as shown in the figure below, is divided into various categories, such as marketing, sales, engineering, quality, human resources, accounting, legal, and administration. We are planning to start Quad Logic with 9 employees by the end of Q4 of 2011. Out of 9 employees, 5 are recruited under the engineering as we will be mainly focusing on development of the 32-bit embedded microprocessor IP till Q2 of 2012. We will be adding ‘4’ development engineers during Q1 of 2012. Since Quad Logic is an IP development company, the IP will need modifications to be customized based on customers’ requirements. Thus, we are planning to retain these 8 core development engineers even after developing the IP as well. Once development is complete, we will be adding more sales team so that we get more customers going forward. However, we are planning to start marketing while the IP is under development itself.

![Organizational Structure Diagram]

Figure 30. Organizational structure
The following table shows the number of employees in each category that is expected to be part of Quad Logic per each year till 2016.

Table 20  Employees

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CEO</td>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SALES and MARKETING</td>
<td>VP of Sales and Marketing</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Marketing Representative</td>
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<td>3</td>
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<td>3</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>Sales Representative</td>
<td>0</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td>ENGINEERING</td>
<td>VP of Engineering</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>DESIGN</td>
<td>Senior Design Engineer</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>Design Engineer</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>VERIFICATION</td>
<td>Senior Verification Engineer</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
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<td></td>
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<td>2</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>APPLICATIONS</td>
<td>Application Engineer</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>QUALITY</td>
<td>Quality Engineer</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>HUMAN RESOURCES</td>
<td>Human Resources Person</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>FINANCE &amp; ACCOUNTANCY</td>
<td>Accountant</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>ADMINISTRATION</td>
<td>Administrator</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>9</td>
<td>20</td>
<td>23</td>
<td>29</td>
<td>35</td>
<td>36</td>
</tr>
</tbody>
</table>

5.12 Business and Revenue Model

Achieving the hypothesis defined in the scope of the project needs a well-defined business plan for Quad Logic, which should include recognizing and defining the
problem, determining the mission and objectives, defining a model, introducing alternative designs, implementing the best design (based on the researches), and finally, testing the design in order to correct the failures and obtain the desired results. The overall planning process of Quad Logic is shown in the figure below.

Figure 31. The overall planning process of Quad Logic

According to the market survey, the major competitors own more than 80% of the high speed embedded control 32-bit microprocessor market around the world (including smart phones and tablet devices market) by selling billion numbers of units. Therefore, Quad Logic is planning to play a key role in this fast paced growing market by following its business plan and its defined vision, mission, goal, and objectives.

5.12.1 Vision
The vision of Quad Logic is to be the first ranked company of Silicon Valley for high speed 32-bit embedded control microprocessors.

5.12.2 Mission
The mission of Quad Logic is to provide high speed 32-bit embedded control microprocessors for various customers with higher performance and comparable price.
5.12.3 Goal
The existing high speed 32-bit embedded microprocessors do not meet the market demands in terms of performance and speed. Therefore, the goal of Quad Logic is to design a 32-bit embedded control microprocessor with better performance, speeds higher than 1 GHz, and comparable price for the manufacturers of various digital devices who use high speed 32-bit embedded control microprocessors for their products.

5.12.4 Objectives
Quad Logic is planning to establish its objectives in the following areas:

- Market share: larger market share, compared to the competitors, to be more profitable
- Innovation: continual research for better 32-bit embedded microprocessor designs in terms of performance, speed, power consumption, and cost that can result in more customer satisfaction compared to the competitors, and more profit for the company
- Productivity and quality: productivity increase and quality improvement with comparable cost for greater customer satisfaction and more profit for the company
- Profitability: continual increase of profitability for company’s survival

5.12.5 Marketing Strategy and Revenue model
Quad Logic is a fab-less Semiconductor Company. The main focus of Quad Logic is IP licensing. Quad Logic is starting with the high performance 32-bit embedded microprocessor IP. This IP is developed in such a way that it is highly configurable based on customers’ requirements. The verification components, such as test suites of this IP, are also developed such that they can be reused at system on chip (SoC) level verification in customers’ verification test bench. Quad Logic delivers the following to customers with each license of the IP:

- Original IP core
- All verification components with the test suite
- All documents related to design and verification
- Integration manual
To get the initial brand name and capture the market of 32-bit embedded microprocessors, we are planning to advertise about the company and the IP while it is in the development phase in major technical journals, business magazines, and technical websites. We will also be participating in technical conferences and webinars to demonstrate our IP.

We would be providing the encrypted core of our IP for evaluation to the customers before their purchase, so that they can evaluate the quality of our IP. This would enable the customers to get more knowledge and direct use with our IP before they purchase the license, so that it would build confidence in customers.

Our main focus is the quality of the IP and the prompt customer support. Once the IP is licensed to any customer, we would be supporting the customer for a minimal annual maintenance cost. We would also be helping them with the integration of our IP in their SoC for free of cost if the customer is paying for the annual maintenance. We are not generally planning to give any modification rights on our IP core to our customers. However, we would like to provide the IP with modification rights as well if it is a potential customer. We are typically planning to charge each license of the IP, which should be used in one product. If any other product group or department in the same company is planning to use our IP, they need to purchase another license of our IP.

For this project, Quad Logic has planned to break even the profit and loss by Q2 of 2013. The initial investment of Quad Logic is $3.2 million. The quarterly profit increases after the breakeven every quarter and would result to 55.8 million dollars by last quarter of 2016 (or in five years). The result will be a return on investment of 177%, which can encourage the investors for investing on our IP.

Quad Logic’s profit is mostly coming from the royalties and NRE. The following table shows the revenue model of Quad Logic from 2011 to 2016. The Revenue model data in the table indicates that Quad Logic makes the profit starting from Q2 of 2013. We are expecting three customers and the minimum of three IP licenses in the year of 2012, which makes us getting the revenues in 2012 onwards.
<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Royalty Rates per Year (in dollars)</th>
<th>Number of Customers (licenses)</th>
<th>Units Sold per year (in thousands)</th>
<th>Royalties (in K$)</th>
<th>NRE (in K$)</th>
<th>Maintenance (in K$)</th>
<th>Revenue (in K$)</th>
<th>Expenses (in K$)</th>
<th>Profit/Loss (in K$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>Q4-2011</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>874</td>
<td>-874</td>
</tr>
<tr>
<td></td>
<td>Q1-2012</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>745</td>
<td>-745</td>
</tr>
<tr>
<td></td>
<td>Q2-2012</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>350</td>
<td>350</td>
<td>828</td>
<td>926</td>
<td>-478</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q3-2012</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>350</td>
<td>70</td>
<td>420</td>
<td>950</td>
<td>-506</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q4-2012</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>350</td>
<td>70</td>
<td>420</td>
<td>950</td>
<td>-530</td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td>Q1-2013</td>
<td>0.85</td>
<td>1</td>
<td>300</td>
<td>255</td>
<td>350</td>
<td>70</td>
<td>675</td>
<td>1073</td>
<td>-398</td>
</tr>
<tr>
<td></td>
<td>Q2-2013</td>
<td>0.85</td>
<td>2</td>
<td>600</td>
<td>510</td>
<td>700</td>
<td>70</td>
<td>1280</td>
<td>1149</td>
<td>131</td>
</tr>
<tr>
<td></td>
<td>Q3-2013</td>
<td>0.85</td>
<td>2</td>
<td>900</td>
<td>765</td>
<td>700</td>
<td>140</td>
<td>1605</td>
<td>1243</td>
<td>362</td>
</tr>
<tr>
<td></td>
<td>Q4-2013</td>
<td>0.85</td>
<td>2</td>
<td>2400</td>
<td>2040</td>
<td>700</td>
<td>140</td>
<td>2880</td>
<td>1238</td>
<td>1642</td>
</tr>
<tr>
<td>2013</td>
<td>Q1-2014</td>
<td>0.6</td>
<td>2</td>
<td>3600</td>
<td>2160</td>
<td>900</td>
<td>140</td>
<td>3200</td>
<td>1417</td>
<td>1783</td>
</tr>
<tr>
<td></td>
<td>Q2-2014</td>
<td>0.6</td>
<td>2</td>
<td>4800</td>
<td>2880</td>
<td>700</td>
<td>180</td>
<td>3760</td>
<td>1405</td>
<td>2355</td>
</tr>
<tr>
<td></td>
<td>Q3-2014</td>
<td>0.6</td>
<td>2</td>
<td>6000</td>
<td>3600</td>
<td>900</td>
<td>140</td>
<td>4640</td>
<td>1561</td>
<td>3079</td>
</tr>
<tr>
<td></td>
<td>Q4-2014</td>
<td>0.6</td>
<td>2</td>
<td>7200</td>
<td>4320</td>
<td>700</td>
<td>180</td>
<td>5200</td>
<td>1563</td>
<td>3637</td>
</tr>
<tr>
<td>2014</td>
<td>Q1-2015</td>
<td>0.5</td>
<td>2</td>
<td>8190</td>
<td>4095</td>
<td>1100</td>
<td>140</td>
<td>5335</td>
<td>1720</td>
<td>3615</td>
</tr>
<tr>
<td></td>
<td>Q2-2015</td>
<td>0.5</td>
<td>2</td>
<td>10080</td>
<td>5040</td>
<td>1100</td>
<td>220</td>
<td>6360</td>
<td>1793</td>
<td>4567</td>
</tr>
<tr>
<td></td>
<td>Q3-</td>
<td>0.5</td>
<td>3</td>
<td>10800</td>
<td>5400</td>
<td>1050</td>
<td>220</td>
<td>6670</td>
<td>1829</td>
<td>4841</td>
</tr>
</tbody>
</table>
Based on the market analysis, we are expecting three customers in the first year (2012) of our IP licensing. The table below shows the customers and the expected licenses. During the first year, we are expecting revenue from NRE alone and not from royalties.

Table 22 Expected number of licenses by Q1-2013

<table>
<thead>
<tr>
<th>Customer</th>
<th>Number of licenses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nokia</td>
<td>1</td>
</tr>
<tr>
<td>Acer</td>
<td>1</td>
</tr>
<tr>
<td>LG</td>
<td>1</td>
</tr>
<tr>
<td>Samsung</td>
<td>1</td>
</tr>
<tr>
<td>Philips</td>
<td>1</td>
</tr>
</tbody>
</table>

The Return on Investment (ROI) is a useful factor to predict the growth of the company. The ROI is used in industry to calculate and estimate the efficiency of an investment. The Return on investment is a difference of total Inflow (Total Revenue) and total Outflow (Total Expenses) divided by total Outflow. The total Inflow is the sum of all the revenues in each quarter/month, whereas the total Outflow is the sum of all the expenses in each quarter/month. The ROI is normally expressed in percentage or a ratio.

\[
\text{ROI (in %)} = \frac{\text{Total Inflow} - \text{Total Outflow}}{\text{Total Outflow}} \times 100
\]
ROI (in %) = \frac{\text{Total Revenue} - \text{Total Expense}}{\text{Total Expense}} \times 100

ROI (in %) = \frac{\text{Total Profit}}{\text{Total Expense}} \times 100

The following table and figure highlight the Return on Investment numbers based on the total revenue (Inflow) and total Expense (Outflow) for every quarter.

Table 23 Quarterly Return on Investment

<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Total Outflow (in K$)</th>
<th>Total Inflow (in K$)</th>
<th>ROI (in %)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>Q4-2011</td>
<td>874</td>
<td>0</td>
<td>-100</td>
</tr>
<tr>
<td>2012</td>
<td>Q1-2012</td>
<td>1619</td>
<td>0</td>
<td>-100</td>
</tr>
<tr>
<td></td>
<td>Q2-2012</td>
<td>2447</td>
<td>350</td>
<td>-86</td>
</tr>
<tr>
<td></td>
<td>Q3-2012</td>
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<td>-77</td>
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<td></td>
<td>Q4-2012</td>
<td>4324</td>
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<td>6546</td>
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<td></td>
<td>Q4-2013</td>
<td>9027</td>
<td>7630</td>
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<td>2014</td>
<td>Q1-2014</td>
<td>10444</td>
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<td></td>
<td>Q2-2014</td>
<td>11848</td>
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<td></td>
<td>Q3-2014</td>
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<td></td>
<td>Q4-2014</td>
<td>14973</td>
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<td>Q2-2015</td>
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<td>36125</td>
<td>95</td>
</tr>
<tr>
<td>Quarter</td>
<td>ROI (in %)</td>
<td>ROI (in %)</td>
<td>ROI (in %)</td>
<td></td>
</tr>
<tr>
<td>---------</td>
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<td></td>
</tr>
<tr>
<td>Q3-2015</td>
<td>20315</td>
<td>42795</td>
<td>111</td>
<td></td>
</tr>
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<td>Q4-2015</td>
<td>22180</td>
<td>49665</td>
<td>124</td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q1-2016</td>
<td>24045</td>
<td>57375</td>
<td>139</td>
<td></td>
</tr>
<tr>
<td>Q2-2016</td>
<td>25910</td>
<td>65370</td>
<td>152</td>
<td></td>
</tr>
<tr>
<td>Q3-2016</td>
<td>27812</td>
<td>73785</td>
<td>165</td>
<td></td>
</tr>
<tr>
<td>Q4-2016</td>
<td>29713</td>
<td>82245</td>
<td>177</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 32. Return on Investment**

Quad Logic is going to breakeven in Q2 of 2013. The Return on Investment by the year 2016 is 177%. The Return on Investment will be improved by putting the right strategies as we move forward.
5.13 Strategic Alliances/Partners
Quad Logic is looking for a strategic partnership with one of the established companies in the microprocessor market for its IP sales in addition to working individually to capture the market share. We would work on the financial strategy together to share the margins on each license of the IP sale. Once our IP captures the market share through the established company, we would also be able to get more customers on our own as our IP would have already been proven in the market by that time.

5.14 Profit and Loss Statement
The following table shows the quarterly profit/loss estimation of Quad Logic from 2011 to 2016. The profit/loss is calculated by subtracting the expenses from revenues. The negative value under profit/loss column represents the loss.

<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Revenue (in K$)</th>
<th>Expenses (in K$)</th>
<th>Profit/Loss (in K$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>Q4-2011</td>
<td>0</td>
<td>874.05</td>
<td>-874.05</td>
</tr>
<tr>
<td>2012</td>
<td>Q1-2012</td>
<td>0</td>
<td>744.96</td>
<td>-744.96</td>
</tr>
<tr>
<td></td>
<td>Q2-2012</td>
<td>350</td>
<td>828.18</td>
<td>-478.18</td>
</tr>
<tr>
<td></td>
<td>Q3-2012</td>
<td>420</td>
<td>926.375</td>
<td>-506.375</td>
</tr>
<tr>
<td></td>
<td>Q4-2012</td>
<td>420</td>
<td>950</td>
<td>-530</td>
</tr>
<tr>
<td>2013</td>
<td>Q1-2013</td>
<td>675</td>
<td>1072.86</td>
<td>-397.86</td>
</tr>
<tr>
<td></td>
<td>Q2-2013</td>
<td>1280</td>
<td>1149.185</td>
<td>130.815</td>
</tr>
<tr>
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<td>Q4-2015</td>
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<td>8460</td>
<td>1901.483</td>
<td>6558.518</td>
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</table>
The following graph shows the quarterly profit/loss estimation of Quad Logic from 2011 to 2015. We will be getting profit from Q2 of 2013 onwards.

Figure 33. Quarterly Profit/Loss Estimate

**5.15 Exit Strategy**

Quad Logic is targeting for more than 10% of the market share in the 32-bit embedded microprocessor market by 2016. To meet this target, we need a total capital investment of $9.0 million till the break even in Q2 of 2013. We are expecting to get an ROI of 177% by the end of 2016. To achieve this ROI, we are planning to analyze regularly on our growth, market share, reputation, brand name, economic uncertainties, etc., for continuous improvement in all aspects. We are looking at the two below exit strategies based on future results.
(1) Merging with a well-established company
(2) Taking Quad Logic to public

6. Conclusion

The market demands a high performance and cost effective solution for various mobile computing requirements. We studied and analyzed the history of the microprocessor and the changes in the architecture over the period of few decades due to the market need in various applications. Applications are getting bigger and need 32-bit embedded processors to handle the large software, which is a big challenge for the designer. Quad Logic’s unique approach, designing a 32-bit embedded control microprocessor, can handle the larger applications by operating at high speeds (over 1GHz) with high performance. The price of our IP is also less than our competitor’s price. Quad Logic’s unique approach to meet the need and economic analysis makes strong and lucrative business case.
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## Appendix A: Instruction Decoder Table

<table>
<thead>
<tr>
<th>DATA PROCESSING OPERATION</th>
<th>PRE-DECODER TABLE</th>
<th>ROM SIGNALS</th>
<th>ALU CONTROLS</th>
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<tr>
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<td>OP CODE</td>
<td>Propagate</td>
<td>A'B'C A'B'C A'B'C A'B'C A'B'C</td>
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</tr>
<tr>
<td></td>
<td>27 26 25 24 23 22 21 20</td>
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<td></td>
<td></td>
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<tr>
<td>AND Op1 AND Op2</td>
<td>0 0 0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0 0</td>
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<td>EOR Op1 - Op2</td>
<td>0 0 0 0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0 0 0</td>
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<td></td>
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<td>ADD Op1 + Op2</td>
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<td></td>
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<tr>
<td>SBC Op1 - Op2 + C</td>
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<td>0 0 0 0 0 0 0 0 0 0</td>
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<td>RSC Op2 - Op1 + C</td>
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| AND Op1 AND Op2           | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| EOR Op1 - Op2             | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| SUB Op1 - Op2             | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| RSB Op2 - Op1             | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| ADD Op1 + Op2             | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| ADC Op1 + Op2 + C         | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| SBC Op1 - Op2 + C         | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| RSC Op2 - Op1 + C         | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| TST set condition codes on Op1 AND Op2 | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| TEQ set condition codes on Op1 EOR Op2 | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| CMP set condition codes on Op1 - Op2 | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| CMN set condition codes on Op1 + Op2 | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| ORR Op1 OR Op2            | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| MOV Rd#=Op2               | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| BIC Rd#=Op1 AND NOT Op2   | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
| MVN Rd#=NOT Op2           | 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 | | |
# Appendix B  Gantt chart

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